Single Phase AC/DC Energy Measurement IC

1. Product Features

Supports measurements of current/voltage RMS values, active power, reactive power, active energy, reactive energy, and other parameters.

- 1U2I mode supporting 2 current channels and 1 voltage channel measurement
- High accuracy:
  - Nonlinear measurement error for active energy < 0.1% within input dynamic range (5000:1)
  - Nonlinear error for voltage/current RMS values < 0.1% within measurement dynamic range (2500:1)
- Configurable filter for input waveforms to obtain full-wave, fundamental wave, or DC RMS values and power
- DC signal measurement capability:
  - Input range: 2000:1
  - Measurement error < ±1%
- Built-in waveform registers for waveform analysis
- Integrated registers for active/reactive energy, current/voltage RMS values
- SPI/UART communication interface
- Anti-creep design to ensure noise cut-off under zero-current conditions
- Power failure monitoring: Chip resets when VDD < 2.7V
- Built-in reference voltage source
- Internal oscillator with ~4MHz clock frequency
- Single 3.3V supply with low power consumption: 15mW (typical)

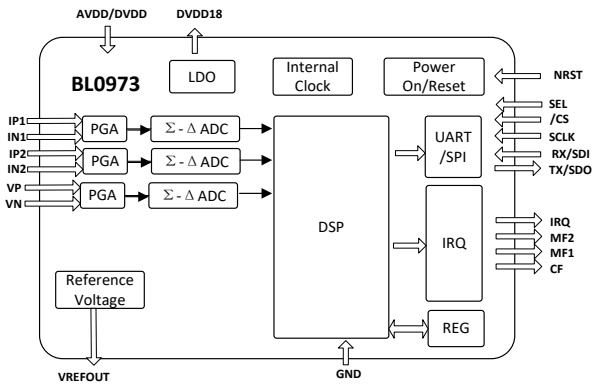
2. Product Applications

- Circuit breakers
- Lighting energy consumption monitoring systems
- Energy meters

3. Product Overview

BL0973 is a single-phase three-channel energy metering chip with an internal clock. It integrates three high-precision Sigma-Delta ADCs, enabling simultaneous measurement of two current channels and one voltage channel.

BL0973 allows users to select different filters for input waveforms to obtain full-wave, fundamental wave, or DC electrical parameters.



Functional Block Diagram

4. Ordering Guide

Product Number	Package	Operating Temp.	Eco Status	MSL	Minimum Pack Qty
BL0973	TSSOP28	-40~85℃	Green	3	3000

Contents

5. Package and Pin Function Description

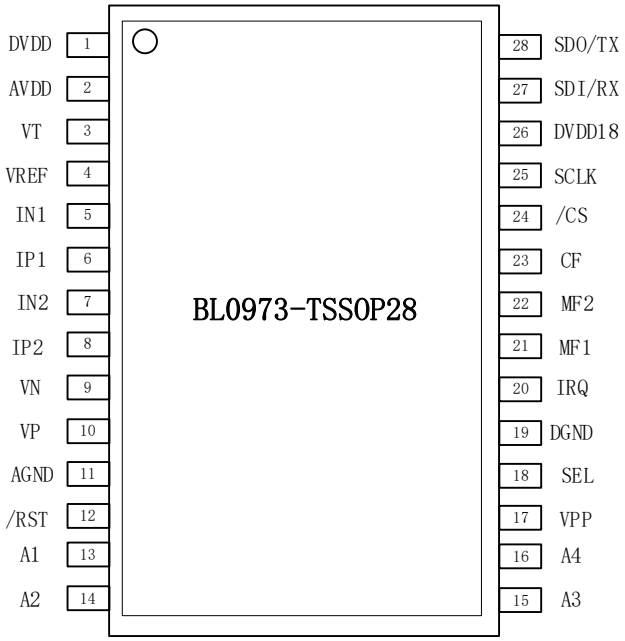


Figure 1 TSSOP28 Pins

Table 1 TSSOP28 Pin Configuration

Pin No	Function	I/O	Description
1	DVDD	I	Digital power supply input (3.3V)
2	AVDD	I	Analog power supply input (3.3V)
3	VT	I	NC
4	VREF	I/O	Reference voltage input/output, connect external 0.1μF filter capacitor
5,6	IN1, IP1	I	Current channel A signal input with adjustable gain (x8~x32). Maximum differential voltage per pin pair: ±175mV pp.
7,8	IN2, IP2	I	Current channel B signal input with adjustable gain (x8~x32). Maximum differential voltage per pin pair: ±175mV pp.
9,10	VN, VP	I	Voltage channel signal input with adjustable gain (x8~x32). Maximum differential voltage per pin pair: ±175mV pp.
11	AGND	I	Ground reference for the analog circuitry.
12	/RST	I	Reset pin (active low)
13	A1	I	Chip address setting for UART interface
14	A2		
15	A3		
16	A4		
17	VPP	I	NC
18	SEL	I	Communication mode selection (SPI/UART)
19	DGND	I	Ground reference for the digital curcuitry

20	/IRQ	O	Interrupt output
21	MF1	O	Logic output
22	MF2	O	Logic output
23	CF	O	Energy calibration pulse output
24	/CS	I	SPI chip select / UART mode baud rate selection
25	SCLK	I	SPI communication clock / UART mode baud rate selection
26	DVDD18	I/O	Digital 1.8V input/output pin, connect external 0.1μF filter capacitor
27	SDI/RX	I	SPI/UART communication pin (data receive)
28	SDO/TX	O	SPI/UART communication pin (data transmit)

6. Product Specifications

6.1 Electrical Parameter Specifications

Table 2 Electrical Parameters

(VDD=3.3V, GND=0V, on-chip voltage reference, built-in crystal oscillator, 25°C, energy measured via the CF output.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active Power Measurement Error	$WATT_{ERR}$	5000：1 input DR		0.1		%
Measurement Error Caused by Inter-Channel Phase Angle						
(PF=0.8 Capacitive)	$PF08C_{ERR}$	Phase Lead 37º		0.1		%
(PF=0.5 Inductive)	$PF05L_{ERR}$	Phase Lag 60º		0.1		%
AC Power Supply Rejection (Output Frequency Amplitude Variation)	AC_{PSRR}	Current Channel Input Pins IP\IN @100mV,		0.01		%
DC Power Supply Rejection (Output Frequency Amplitude Variation)	DC_{PSRR}	Voltage Channel Input Pins VP\VN=100mV		0.1		%
Voltage RMS Measurement Accuracy, Relative Error	$VRMS_{ERR}$	2500：1 input DR		0.1		%

Current RMS Measurement Accuracy, Relative Error	$IRMS_{ERR}$	2500：1 input DR		0.1		%
Analog Input						
Input Level (Peak)		Differential Input			175	mV
Input Impedance				37		kΩ
Bandwidth (-3dB)				14		kHz
Gain Error		External 1.2V Reference Voltage		0.5		%
Inter-Phase Gain Matching Error		External 1.2V Reference Voltage		0.3		%
Internal Voltage Reference	Vref			1.0975		V
Reference Deviation	$Vref_{ERR}$			5		mV
Temperature Coefficient	TempCoef			20		ppm/℃
Logic Input						
SDI, SCLK, /CS						
Input High Level		VDD=3.3V±2.5%	2.6			V
Input Low Level		VDD=3.3V±2.5%			0.8	V
Logic Output						
SDO, DO1, DO2, CF, /IRQ						
Output High Level		VDD=3.3V±2.5%	2.6			V
Output Low Level		VDD=3.3V±2.5%			1	V
Power Supply						
VDD	V_{VDD}		3	3.3	3.6	V
DVDD18	V_{DVDD18}	VDD18=1.8V	1.62	1.8	1.98	V
IDD	I_{VDD}	VDD=3.3		4	6	mA

6.2 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings (T = 25℃)

Item	Symbol	Limit	Unit
Supply Voltage VDD	VDD	-0.3 ~ +4	V
Supply Voltage DVDD18	DVDD18	-0.3 ~ +2.5	V
Analog Input Voltage (relative to AGND)	IN1、IP1、IN2、IP2、VP、VN、VT	-1 ~ +VDD	V
Analog Output Voltage (relative to AGND)	Vref	-0.3 ~ +VDD	V
Digital Input Voltage (relative to DGND)	/SDI、SCLK、/CS	-0.3 ~ VDD+0.3	V
Digital Output Voltage (relative to DGND)	CF、MF1、MF2、SDO、/IRQ	-0.3 ~ VDD+0.3	V
Operating Temperature	Topr	-40 ~ +85	℃
Storage Temperature	Tstr	-55 ~ +150	℃

7. Detailed Description

7.1 Operating Principle

7.1.1 Current and Voltage Waveform Generation Principle

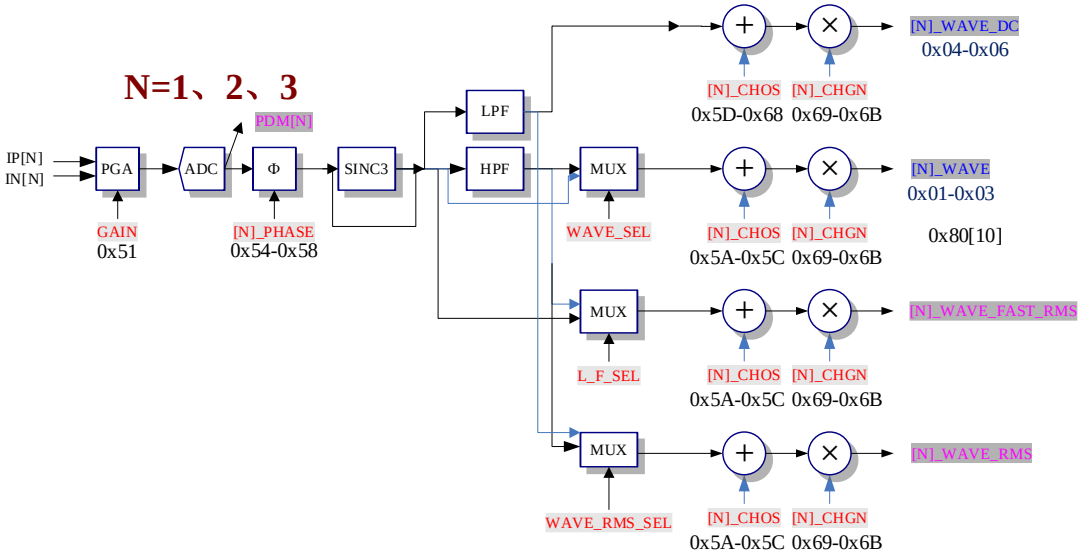


Figure 2 Waveform Generation Signal Chain

As shown in the figure above, three identical high-precision ADCs with differential input structures are employed: the current channel and voltage channel respectively receive positive/negative voltage signals IP1, IN1, IP2, IN2, and VP, VN.

Within each channel, the input signals pass through a programmable gain amplifier (PGA) in the analog module and a high-precision analog-to-digital converter (ADC). The converted PDM codes are then transmitted to the digital module.

The digital module processes the data through phase calibration, a decimation filter (SINC3), an optional high-pass filter (HPF) or DC-blocking low-pass filter (LPF), followed by gain and offset correction modules. This yields the required current waveform data (IA_WAVE, IB_WAVE) and voltage waveform data (V_WAVE).

7.1.1.1 PGA Gain Adjustment

The PGA gains of both current and voltage channels are adjustable. The data format of the PGA gain adjustment register (GAIN) is as follows: (Each 4-bit field controls one channel: 0010 = 8; 0011 = 16; 0110 = 24; 0111 = 32).

Table 4 PGA Gain Adjustment Register

Addr	Name	Width	Default Value	Description
51	GAIN	12	0x000	PGA Channel Gain Adjustment Register: [3:0]: Voltage channel; [7:4]: Current B channel; [11:8]: Current A channel

7.1.1.2 Channel Offset Calibration

Includes three 16-bit channel offset calibration registers CHOS as follows, with a default value of 0x0000.

These registers use two's complement format data to eliminate the deviations introduced by analog-to-

digital conversion in current and voltage channels respectively. The deviations may originate from input signals or the inherent offset of the ADC circuit itself. Offset calibration ensures zero waveform offset under no-load conditions.

Table 5 Channel Offset Adjustment Register

Addr	Name	Bit Width	Default Value	Description
5A	IA_CHOS	16	0x0000	Current Channel A Offset Adjustment Register, two's complement
5B	IB_CHOS	16	0x0000	Current Channel B Offset Adjustment Register, two's complement
5C	V_CHOS	16	0x0000	Voltage Channel Offset Adjustment Register, two's complement

Bias Adjustment Calibration Formula:

$$WAVE = WAVE0 + CHOS$$

where WAVE0 is the measured value of the channel, and WAVE is the calibrated output value.

7.1.1.3 Channel Gain Calibration

Includes three 16-bit channel gain calibration registers CHGN as follows, with a default value of 0x0000.

Table 6 Channel Gain Adjustment Register

Addr	Name	Bit Width	Default Value	Description
69	IA_CHGN	16	0x0000	Current Channel A Gain Adjustment Register, two's complement
6A	IB_CHGN	16	0x0000	Current Channel B Gain Adjustment Register, two's complement
6B	V_CHGN	16	0x0000	Voltage Channel Gain Adjustment Register, two's complement

These registers use two's complement format data to compensate for gain errors introduced by the current and voltage channel analog-to-digital conversions. Such errors may originate from input sources or the ADC circuitry itself. The gain calibration allows adjustments within a range of ±50%.

Channel Gain Calibration Formula:

$$\mathrm{WAVE} = \mathrm{WAVE0} * (1 + \frac{\mathrm{CHGN}}{2^{16}})$$

where WAVE0 is the measured value of the channel and WAVE is the calibrated output value.

7.1.1.4 Current/Voltage Waveform Output

Capable of acquiring real-time load current and voltage waveform data. The sampled current and voltage values are updated at approximately 15ksps, with 300 points sampled per waveform cycle. Each sampled data point is a 24-bit signed value stored in dedicated waveform registers (IA_WAVE, IB_WAVE, V_WAVE).

Table 7 Waveform Registers

Addr	Name	Bit Width	Default Value	Description
1	IA_WAVE	24	0x000000	Current Channel A Waveform Register
2	IB_WAVE	24	0x000000	Current Channel B Waveform Register
3	V_WAVE	24	0x000000	Voltage Channel Waveform Register
4	IA_WAVE_DC	24	0x000000	Current A DC Waveform Register
5	IB_WAVE_DC	24	0x000000	Current B DC Waveform Register
6	V_WAVE_DC	24	0x000000	Voltage DC Waveform Register

The current waveform output selection can be configured through the user mode register MODE[10]. The voltage waveform output is the normal waveform (the waveform used for RMS calculation).

Table 8 Current Waveform Selection

0x44	MODE1	Operation Mode Register	
No.	name	default value	description
[10]	WAVE_REG_SEL	1'b0	Current waveform register output selection: Default 0 selects waveform from normal current channel. 1 selects waveform output from fast measurement channel

The normal waveform (for RMS calculation) is categorized into AC, DC, and full-wave modes. When using HPF, it operates in AC measurement mode and outputs the AC waveform. When using LPF (Low-Pass Filter) for DC measurement mode, it outputs the DC waveform. After SINC filtering, the full-wave waveform is obtained, which can be configured via the user mode register MODE.

Table 9 RMS waveform selection

0x44	MODE	Operation Mode Register	
No.	name	default value	description
[9:4]	WAVE_RMS_SEL	2'b00	RMS waveform selection: 00-HPF, 10-DC, 01-SINC, 11-HPF [9:8]: Voltage channel; [7:6]: Current B channel; [5:4]: Current A channel

The waveform of the fast measurement channel (used for fast RMS calculation) is divided into full-wave and AC full-wave modes. Full-wave waveform is output without passing through the HPF (High Pass Filter). AC measurement mode outputs AC full-wave waveform when passing through the HPF. This can be configured via the user mode register MODE[0].

Table 10 Fast measurement selection

0x44	MODE1	Operation Mode Register	
No.	name	default value	description
[0]	L_F_SEL	1'b0	Fast measurement selection via HPF, 0-full wave (default), 1-AC full wave

7.1.2 Active Power Calculation Principle

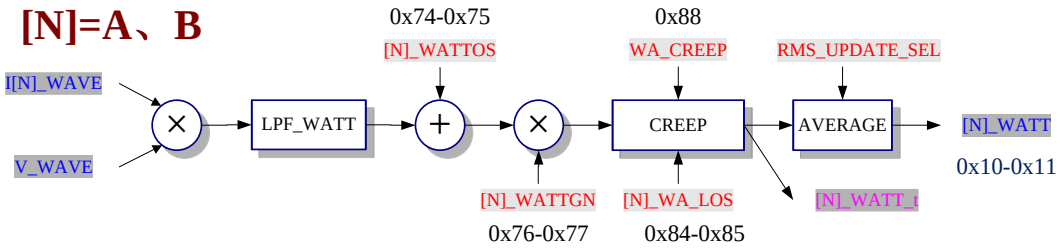


Figure 3 Active Power Signal Chain

The power signal is obtained by digitally multiplying current and voltage waveforms, followed by sequential processing through a low-pass filter, gain and offset calibration, anti-creep judgment, and averaging.

7.1.2.1 Selection of Active Waveform

The waveforms used for power calculation can be configured via the user mode register MODE.

Note: When calculating DC power, both current and voltage waveforms must be selected as DC for power computation.

Table 11 Active Power waveform selection

0x44	**MODE**	**Operation Mode Register**	
No.	**name**	**default value**	**description**
[3:1]	WAVE_SEL	1'b0	Active power waveform selection: 0-AC, 1-DC

7.1.2.2 Active Power Output

The active power register is a 24-bit signed number in two's complement format. Bit[23] is the sign bit, indicating positive/negative power.

Table 12 Active Power Registers

Addr	**Name**	**Bit Width**	**Default Value**	**Description**
10	A_WATT	24	0x000000	Channel A active power, two's complement format
11	B_WATT	24	0x000000	Channel B active power, two's complement format

7.1.2.3 Active Power Calibration

There are two 16-bit active power offset correction registers (WATTOS) and two 16-bit active power gain correction registers (WATTGN), with default values of 0x0000.

WATTOS is used to eliminate DC offset in active power calculations, while WATTGN compensates for gain deviation in active power calculations. These deviations may originate from crosstalk between channels on the PCB or within the integrated circuit itself, or from inherent ADC channel gain mismatch.

Offset correction ensures that the active power register value approaches zero under no-load conditions.

Table 13 Active Power Adjustment Registers

Addr	**Name**	**Bit Width**	**Default Value**	**Description**
76	A_WATTGN	16	0x0000	Active power gain adjustment for Channel A, two's complement

77	B_WATTGN	16	0x0000	Active power gain adjustment for Channel B, two's complement
74	A_WATTOS	16	0x0000	Active power offset adjustment for Channel A, two's complement
75	B_WATTOS	16	0x0000	Active power offset adjustment for Channel B, two's complement

Correction result of active power:

$$WATT = WATT0 * (1 + \frac{WATTGN}{2^{16}})$$

where WATT is the corrected active power, and WATT0 is the active power before correction.

7.1.2.4 Phase Compensation

The ADC output stage incorporates a digital calibration method for minor phase errors. It introduces a small time delay or advance into the signal processing circuit to compensate for slight phase deviations. Since this compensation must occur in-time, it is only applicable for minor phase errors within <0.6°. Using time-shift techniques to correct large phase errors would introduce significant phase distortions in higher-order harmonics.

The phase compensation for current and voltage channels is adjustable. The data format of the phase calibration register PHASE is as follows (each 8 bits calibrate one channel: [7] is reserved, [6:0] has a minimum adjustment delay of 250ns, corresponding to 0.0045 degrees/1LSB, with a maximum adjustable range of ±0.5715 degrees).

Table 14 phase calibration registers

Addr	Name	Bit Width	Default Value	Description
52	IRMS_P1	16	0x0100	Phase angle segmentation point P1 definition, satisfying IRMSmin < P1 < P2 < IRMSmax
53	IRMS_P2	16	0x2000	Phase angle segmentation point P2 definition, satisfying IRMSmin < P1 < P2 < IRMSmax
54	IA_PHCAL1	16	0x0000	Current channel A phase calibration register 1. When IRMSmin < input current RMS < P1, [6:0] corrects current channel phase. When P1 < input current RMS < P2, [14:8] corrects current channel phase.
55	IA_PHCAL2	8	0x00	Current channel A phase calibration register 2. When P2 < input current RMS < IRMSmax, [6:0] corrects current channel phase.
56	IB_PHCAL1	16	0x0000	Current channel B phase calibration register (same as address 54)
57	IB_PHCAL2	8	0x00	Current channel B phase calibration register (same as address 55)
58	V_PHCAL	8	0x00	Voltage channel phase calibration register (same as address 53)

7.1.2.5 Anti-Creep for Active Power

The chip integrates a patented anti-creep power module to ensure zero power output when no current is input.

The active anti-creep threshold register (WA_CREEP) is a 12-bit unsigned value with a default setting of 0x04C. This value is multiplied by 2 and then compared with the absolute value of the input active power signal. If the absolute value of the input active power signal is smaller than this threshold, the output active power is forced to zero. This ensures that, under no-load conditions, even with minor noise signals, the active power register output remains 0.

Table 15 anti-creep threshold register

Addr	Name	Bit Width	Default Value	Description
88	WA_CREEP	12	0x04C	Active Power Anti-Creep Threshold

When the chip is in anti-creep mode, power values below the threshold are excluded from energy accumulation.

7.1.2.6 Small-Signal Compensation for Active Power

For active power calculation, the small-signal compensation register can be used to adjust nonlinear errors in the small-signal range, thereby reducing noise-induced errors.

The active power small-signal compensation register (WA_LOS) is a 12-bit two's complement value with a default setting of 0x000.

Table 16 small-signal compensation registers

Addr	Name	Bit Width	Default Value	Description
84	A_WA_LOS	12	0x000	Channel A Active Power Small-Signal Compensation, Two's Complement
85	B_WA_LOS	12	0x000	Channel B Active Power Small-Signal Compensation, Two's Complement

7.1.3 Active Energy Measurement Principle

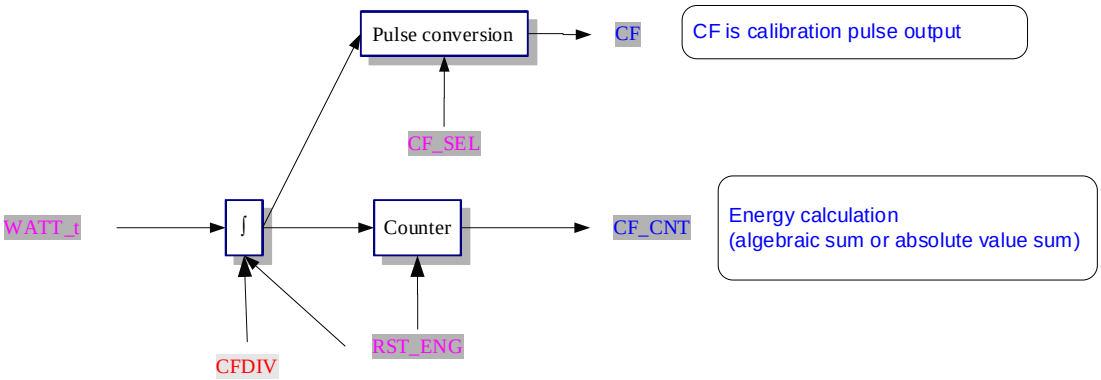


Figure 4 Active Energy Signal Chain

By integrating active power over a period of time, the active energy during that period can be obtained. This energy is further converted into corresponding frequency calibration pulses (CF). The more

electricity is consumed, the faster the CF frequency; the less electricity is consumed, the slower the CF frequency.

7.1.3.1 Active Energy Output

The energy (electricity consumption) can be obtained by counting CF pulses, which are stored in the energy pulse accumulation register X_CF_CNT.

Table 17 Active Energy Pulse Counters

Addr	Name	Bit Width	Default Value	Description
26	A_CF_CNT	24	0x000000	Channel A Active Energy Pulse Counter (Unsigned)
27	B_CF_CNT	24	0x000000	Channel B Active Energy Pulse Counter (Unsigned)

The active energy register is used to store the continuously accumulated active energy.

Table 18 Accumulated Active Energy Registers

Addr	**Name**	**Bit Width**	**Default Value**	**Description**
1C	A_WATTHR	24	0x000000	Channel A Active Energy Accumulation (Unsigned)
1D	B_WATTHR	24	0x000000	Channel B Active Energy Accumulation (Unsigned)

7.1.3.2 Active Energy Output Selection

The CF pulse output representing energy information can be configured via MODE_OUT.

Table 19 CF Output Channel Selection

0x43	**MODE_OUT**	**Operation Mode Register**	
No.	**name**	**default value**	**description**
[7:4]	CF_SEL	4'b0000	CF Output Channel Selection: 0000-Default (CF output disabled); 0001-A_CF; 0010-B_CF; 0011-A_CFQ; 0100-B_CFQ; 0101-A_CF_DC; 0110-B_CF_DC; 0111-A_CFS; 1000-B_CFS; 1001-A_CF_SUM; 1010-B_CF_SUM;

MODE[11] (CF_ADD_SEL) can be used to set the energy accumulation method: algebraic sum or absolute value sum.

The counting results of CF pulses are stored in the corresponding pulse counting registers. The CF pin can also be configured to output meter calibration pulses. When the CF pulse period is less than 180ms, it outputs a 50% duty cycle pulse. When the period is greater than or equal to 180ms, the high-level duration is fixed at 90ms.

7.1.3.3 Active Energy Output Scaling

During energy accumulation, the accumulation rate can be adjusted through the CF_DIV register with 12 gear settings, each having a 2x relationship (coarse adjustment).

Table 20 CF Scaling Factor Register

Addr	Name	Bit Width	Default Value	Description
A2	CFDIV	12	0x010	CF Scaling Factor Register

Taking the default value 0x010 as the reference pulse output, the output pulse frequency ratios relative to CFDIV=0x010 for other settings are as follows.

Table 21 CF Scaling Factor

CFDIV	Scaling Factor	CFDIV	Scaling Factor
0x000	0.03125	0x040	4
0x001	0.0625	0x080	8
0x002	0.125	0x100	16
0x004	0.25	0x200	32
0x008	0.5	0x400	64
0x010	1	0x800	256
0x020	2		

The relationship between pulse period and CFDIV/WATT register values is given by the formula:

$$t_{CF} = \frac{4194304 \times 0.032768 \times 32}{CFDIV \times WATT}$$

7.1.4 Current and Voltage RMS Calculation Principle

The RMS calculation principle for channels is illustrated in the figure below.

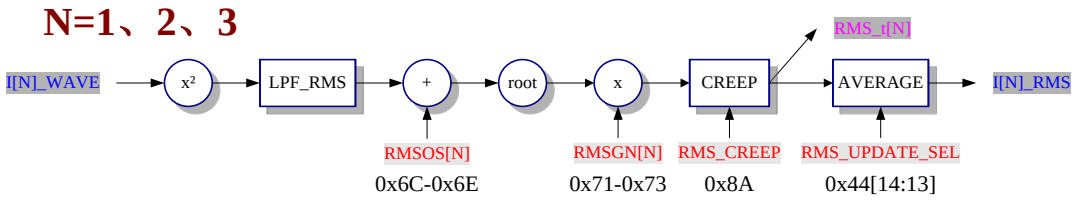


Figure 5 RMS calculation Signal Chain

The original waveform of the channel is processed through a squaring circuit (X²), an RMS low-pass filter (LPF_RMS), and a square root circuit (ROOT) to obtain the instantaneous RMS value (RMS_t). This value is then averaged to derive the mean RMS values for current (I_RMS) and voltage (V_RMS).

7.1.4.1 RMS Output

The RMS calculation results are stored in the RMS register, which is a 24-bit unsigned value.

Table 22 RMS Register

Addr	Name	Bit Width	Default Value	Description
7	IA_RMS	24	0x000000	Current Channel A RMS Register (Unsigned)
8	IB_RMS	24	0x000000	Current Channel B RMS Register (Unsigned)
9	V_RMS	24	0x000000	Voltage Channel RMS Register (Unsigned)

When a channel enters the anti-creep state for RMS measurement, the value of its RMS register is forced to zero and stops updating.

7.1.4.2 RMS Input Signal Configuration

The waveform for RMS calculation can be configured as Full-wave, AC full-wave, or DC. The full-wave waveform is output without passing through the HPF. In AC measurement mode (with HPF enabled), the AC full-wave waveform is output. In DC measurement mode (with LPF enabled for DC extraction), the DC waveform is output. These modes can be configured via the user-mode register MODE.

Table 23 RMS waveform selection

0x44	**MODE**	**Operation Mode Register**	
No.	**name**	**default value**	**description**
[9:4]	WAVE_RMS_SEL	2'b00	RMS waveform selection: 00-HPF, 10-DC, 01-SINC, 11-HPF [9:8]: Voltage channel; [7:6]: Current B channel; [5:4]: Current A channel

7.1.4.3 RMS Refresh Rate Setting

By configuring the RMS_UPDATE_SEL bits in MODE[14:13], the average refresh time for RMS values can be selected.

Table 24 RMS register update rate selection

0x44	**MODE**	**Operation Mode Register**	
No.	**name**	**default value**	**description**
[14:13]	RMS_UPDATE_SEL	2'b00	RMS register update rate selection, 11-1000ms, 00-500ms (default), 01-250ms, 10-125ms

7.1.4.4 Current/Voltage RMS Calibration

Two 24-bit RMS offset correction registers (RMSOS) with a default value of 0x000000 (two's complement). Two 16-bit RMS gain correction registers (RMSGN) with a default value of 0x0000 (two's complement).

These registers are used to calibrate deviations in RMS calculations. Such deviations may originate from input noise, as the RMS calculation involves a squaring operation that could introduce DC offsets caused by noise. Gain and offset corrections ensure the RMS register values approach 0 under no-load conditions.

Table 25 RMS adjustment

Addr	**Name**	**Bit Width**	**Default Value**	**Description**
6C	IA_RMSOS	16	0x0000	Current channel A RMS offset adjustment, two's complement
6D	IB_RMSOS	16	0x0000	Current channel B RMS offset adjustment, two's complement
6E	V_RMSOS	16	0x0000	Voltage channel RMS offset adjustment, two's complement
71	IA_RMSGN	16	0x0000	Current channel A RMS gain adjustment, two's

				complement
72	IB_RMSGN	16	0x0000	Current channel B RMS gain adjustment, two's complement
73	V_RMSGN	16	0x0000	Voltage channel RMS gain adjustment, two's complement

RMS Offset Calibration Formula:

$$RMS = \sqrt{{RMS_0}^2 + RMSOS \times 1024}$$

RMS Gain Calibration Formula:

$$RMS = RMS0 * (1 + \frac{RMSGN}{2^{16}})$$

where RMS0 represents the RMS value before channel calibration, and RMS is the RMS value after channel calibration.

The adjustment range of RMSGN is ±50%.

7.1.4.5 RMS Anti-Creep Function

Equipped with patented RMS anti-creep technology to ensure zero RMS output when no current is input.

The RMS anti-creep threshold register (RMS_CREEP) is a 12-bit unsigned value, defaulting to 0x200.

This value is multiplied by 2 and compared with the absolute value of the input RMS signal. If the input RMS signal is smaller than this threshold, the output RMS is forced to zero. This ensures that, under no-load conditions, even in the presence of minor noise signals, the value written to the RMS register remains zero.

Table 26 RMS Small Signal Threshold Register

Addr	Name	Bit Width	Default Value	Description
8A	RMS_CREEP	12	0x200	RMS Small Signal Threshold Register

7.1.5 Principle of Fast RMS Detection

The principle of fast RMS calculation is illustrated in the figure below.

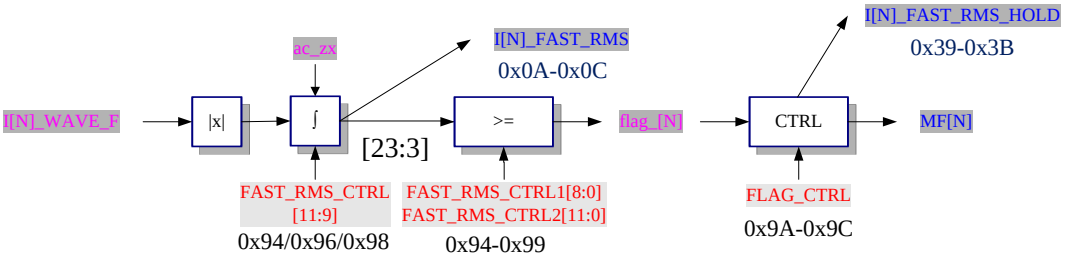


Figure 6 Fast RMS calculation Signal Chain

The current channel features a fast RMS register capable of detecting half-cycle or full-cycle RMS values. This function can be used for leakage current or overcurrent detection.

The input waveform undergoes absolute value processing, followed by integration over a specified time period to obtain the fast RMS value. This value I_FAST_RMS[23:3] is compared with a preset threshold FAST_RMS_CTRL[20:0]. If exceeded, a flag can be triggered.

7.1.5.1 Fast RMS Output

The fast RMS output registers for current and voltage channels are as follows. These registers are 24-bit unsigned values.

Table 27 Fast RMS Register

Addr	Name	Bit Width	Default Value	Description
A	IA_FAST_RMS	24	0x000000	Current Channel A Fast RMS Register
B	IB_FAST_RMS	24	0x000000	Current Channel B Fast RMS Register
C	V_FAST_RMS	24	0x000000	Voltage Channel Fast RMS Register

7.1.5.2 Fast RMS Input Selection

The waveforms for fast RMS calculation include full-wave and AC full-wave. The full-wave waveform is output without passing through the HPF.

When using the HPF, it operates in AC measurement mode, outputting the AC full-wave waveform. This can be configured via the user mode register MODE[0].

Table 28 Fast measurement selection

0x96	MODE1	Operation Mode Register	
No.	name	default value	description
[0]	L_F_SEL	1'b0	Fast measurement selection via HPF. Default 0-No HPF (full wave), 1-HPF selected (AC full wave)

7.1.5.3 Fast RMS Accumulation Time and Threshold

For fast RMS calculation, the absolute value is first taken, followed by integration based on the preset accumulation time. Typically, integer multiples of half-cycle or full-cycle durations are selected.

Table 29 Fast RMS Accumulation Time and Threshold

Addr	Name	Bit Width	Default Value	Description
94	IA_FAST_RMS_CTRL1	12	0x20F	[11:9] Refresh time for the channel's fast RMS register. Options include half-cycle or N full cycles. The default is one full cycle; [8:0] Upper bits [20:12] of the channel's fast RMS threshold.
95	IA_FAST_RMS_CTRL2	12	0xFFF	Lower bits [11:0] of the channel's fast RMS threshold.
96	IB_FAST_RMS_CTRL1	12	0x20F	[11:9] Refresh time for the channel's fast RMS register. Options include half-cycle or N full cycles. The default is one full cycle; [8:0] Upper bits [20:12] of the channel's fast RMS threshold.
95	IB_FAST_RMS_CTRL2	12	0xFFF	Lower bits [11:0] of the channel's fast RMS threshold.
97	V_FAST_RMS_CTRL1	12	0x20F	[11:9] Refresh time for the channel's fast RMS register. Options include half-cycle or N full cycles. The default is one full cycle; [8:0] Upper bits [20:12]

				of the channel's fast RMS threshold.
95	V_FAST_RMS_CTRL2	12	0xFFF	Lower bits [11:0] of the channel's fast RMS threshold.

The accumulation time is configured via FAST_RMS_CTRL1[11:9], with six options: 000 – 10ms, 001 – 20ms, 010 – 40ms, 011 – 80ms, 100 – 160ms, 101 – 320ms. By default, the full-cycle accumulation response time of 20ms is selected. A longer accumulation time results in smaller fluctuations.

FAST_RMS_CTRL1[8:0] | FAST_RMS_CTRL2[11:0] is used to set the fast RMS over-limit threshold. Once the fast RMS register value [23:3] exceeds this threshold, the output flag (flag) is set to 1. This flag is connected to the output (MF) and can directly pull the overcurrent indication pin high. It can be used in conjunction with the overcurrent indication control register.

7.1.5.4 Power Grid Frequency Selection

The AC_FREQ_SEL register allows selection between 50Hz and 60Hz power grid applications.

Table 30 AC frequency selection

0x44	**MODE**	**Operating Mode Register**	
No.	**name**	**default value**	**description**
[15]	AC_FREQ_SEL	1'b0	AC frequency selection: 1 = 60 Hz 0 = 50 Hz (default is 50 Hz)

7.1.5.5 Fast RMS Overlimit Data Storage

To record fast overload signals, the fast RMS overlimit feature includes data retention functionality. Specific register operations are required to clear the related FAST_RMS_HOLD registers. Refer to the following table for details:

Table 31 Fast RMS Register

Addr	**Name**	**Bit Width**	**Default Value**	**Description**
39	IA_FAST_RMS_HOLD	24	0x000000	Current Channel A Fast RMS Register, unsigned, hold
3A	IB_FAST_RMS_HOLD	24	0x000000	Current Channel B Fast RMS Register, unsigned, hold
3B	IA_FAST_RMS_HOLD	24	0x000000	Voltage Channel Fast RMS Register, unsigned, hold

7.1.5.6 Overcurrent Indication

The overcurrent indication (MF) can be controlled through the following overcurrent indication control registers:

Table 32 Overcurrent indication control register

Addr	**Name**	**Bit Width**	**Default Value**	**Description**
9B	flag_ctrl1	16	0x0000	Overcurrent indication control register 1
9C	flag_ctrl2	16	0x0000	Overcurrent indication control register 2

7.1.5.7 Relay Control

The output level of the MF pin can also be directly controlled by writing to the flag_ctrl register to control relays:

Table 33 Relay Control

Addr	Name	Bit Width	Default Value	Description
9A	flag_ctrl	12	0x000	[11:9]: Master control selection for MF3–MF1: 0 = output internal indicator; 1 = directly controlled by master [8:6]: Output level of MF3–MF1 when directly controlled by master [5:3]: Indicator selection for MF3–MF1: 0 = output real-time interrupt; 1 = output delayed control [2:0]: Delay control for MF3–MF1=0: 0 = Disable, 1 = Enable

7.1.6 Electrical Parameter Measurement

7.1.6.1 Line Frequency Measurement

The grid frequency is measured through the voltage channel.

The count value recorded in the PERIOD register corresponds to the line voltage cycle period. If the input signal deviates from 50Hz/60Hz, the corresponding count value will change.

Table 34 Line voltage frequency/period register

Addr	Name	Bit Width	Default Value	Description
35	PERIOD	20	0x000000	Line voltage frequency/period register

7.1.6.2 Phase Angle Calculation

The principle of phase angle measurement is illustrated in the figure below.

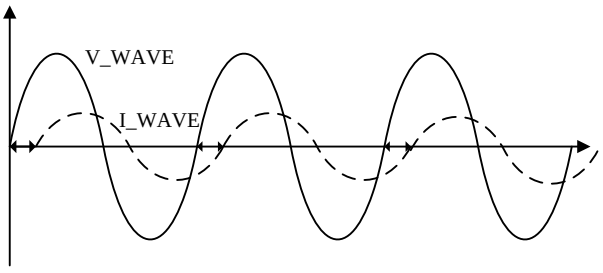


Figure 7 phase angle measurement

The phase difference is obtained by calculating the time interval between the positive zero-crossings of current and voltage. The corresponding time value is updated to the ANGLE register, which is a 16-bit unsigned number.

Table 35 AC frequency selection

Addr	Name	Bit Width	Default Value	Description
36	A_CORNER	16	0x0000	Phase angle register between current A and voltage waveforms
37	B_CORNER	16	0x0000	Phase angle register between current B and voltage waveforms

7.1.6.3 Power Sign Bit

For the power pulse CF output, there is a sign bit register that indicates the direction of CF. This direction signifies whether the corresponding accumulated energy during the period from the previous CF pulse to the current CF pulse is in the power consumption or power generation direction.

Table 36 Power Sign Bit Register

Addr	Name	Bit Width	Default Value	Description
30	SIGN	10	0x000	Sign bit corresponding to the current energy pulse count, refreshed upon each CF pulse output.

7.1.7 Fault Detection

7.1.7.1 Zero-Crossing Detection

Voltage zero-crossing detection is provided. When zx is 0, it indicates the positive half-cycle of the waveform; when zx is 1, it indicates the negative half-cycle. The output is a fundamental zero-crossing signal that has passed through a HPF filter, introducing a delay of approximately 570us compared to the actual input signal.

The zero-crossing signal is primarily used to assist in disconnecting the relay at the zero-crossing point, which helps reduce relay sticking.

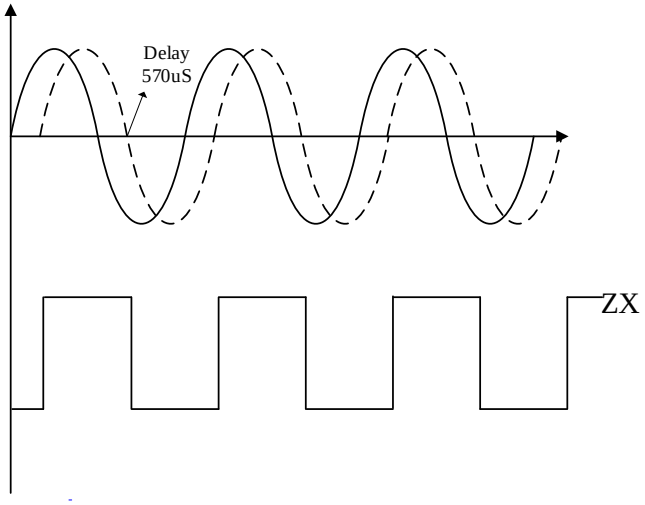


Figure 8 Zero-Crossing Detection

Note: To prevent uncertainties caused by stray signals from background noise or small signals, the current zero-crossing threshold is set to 70,000, and the voltage zero-crossing threshold is 200,000. If the instantaneous RMS value is smaller than the threshold, the ZX signal will be uncertain.

The zero-crossing signal output is configured as /ZX (ZX inverted) via the /IRQ pin.

7.1.7.2 Peak Overlimit

Threshold values for current and voltage RMS can be set via peak threshold registers (I_PKLVL, V_PKLVL).

Table 37 peak threshold register

Addr	Name	Bit Width	Default Value	Description
8C	V_PKLVL	16	0xFFFF	[15:12]: Number of consecutive half-cycles for detection [11:0]: Voltage peak threshold register V_PKLVL
8D	I_PKLVL	16	0xFFFF	[15:12]: Number of consecutive half-cycles for detection [11:0]: Current peak threshold register I_PKLVL

For example: when the current fast RMS exceeds the threshold set in the current peak threshold register (I_PKLVL), a current overload indication PKI is triggered. If the corresponding PKI enable bit in the interrupt mask register (MASK) is set to logic 0, the /IRQ logic output becomes active low.

Similarly, when the voltage fast RMS exceeds the threshold set in the voltage peak threshold register (V_PKLVL), a voltage overload indication PKV is triggered. If the corresponding PKV enable bit in the interrupt mask register (MASK) is set to logic 0, the /IRQ logic output becomes active low.

Table 38 peak overlimit signal

0x3F	STATUS		
Position	**Interrupt Flag**	**Default Value**	**Description**
5	PK_IA	0	Current Channel A peak overlimit signal
6	PK_IB	0	Current Channel B peak overlimit signal
7	PK_V	0	Voltage channel peak overlimit signal

7.1.7.3 Line Voltage Sag

A line voltage sag indication is triggered when the RMS value of the line voltage remains below a certain threshold for more than a specified number of half cycles.

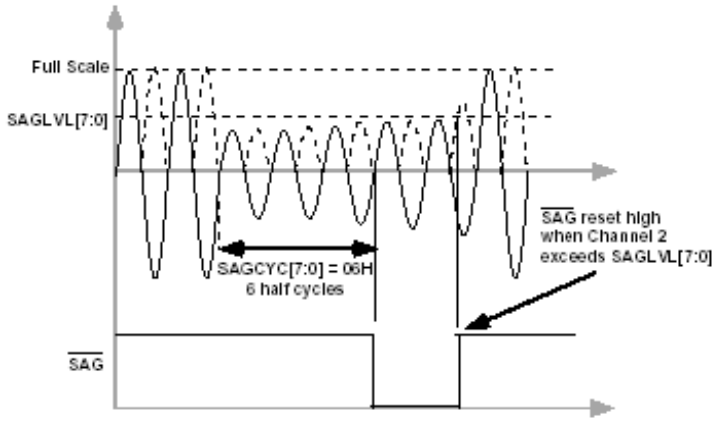


Figure 9 Sag Detection

As shown in the figure above, when the voltage RMS falls below the threshold set in the sag voltage threshold register (SAGLVL) and the duration exceeds the time configured in the sag line cycle register

(SAGCYC) (illustrated as exceeding the 6th half cycle, where SAGCYC[11:0] = 06H), the line voltage sag event is recorded by setting the SAG flag in the interrupt status register (STATUS).

Table 39 Line voltage sag register

0x3F	**STATUS**		
Position	**Interrupt Flag**	**Default Value**	**Description**
3	SAG	0	Line voltage sag detected

If the corresponding SAG enable bit in the interrupt mask register (MASK) is set to logic 0, the /IRQ output becomes active low.

The sag cycle count and sag voltage threshold can be configured. The sag voltage threshold register (SAGLVL) allows user read/write access with a default value of 0x100, while the sag line cycle register (SAGCYC) also supports user read/write operations with a default value of 0x04.

Table 40 Sag cycle count and Sag voltage threshold register

Addr	**Name**	**Bit Width**	**Default Value**	**Description**
91	SAGCYC	8	0x04	Sag cycle count (SAGCYC)
92	SAGLVL	12	0x100	Sag voltage threshold register (SAGLVL). If the voltage channel input remains continuously below this threshold for longer than the duration specified in SAGCYC, a line voltage sag interrupt will be triggered. Default value is 0x100.

7.1.7.4 Zero-Crossing Timeout

The zero-crossing detection circuit is connected to a timeout detection register ZXTOUT. Each time a zero-crossing signal is detected on the voltage channel, ZXTOUT is reset to its initial value. If no zero-crossing signal is detected, the register value decrements. If no zero-crossing signal is output for an extended period, the register value will reach 0, at which point the corresponding ZXTO bit in the interrupt status register is set to 1. If the corresponding enable bit ZXTO in the interrupt mask register is set to 0, the zero-crossing timeout event will also be reflected on the interrupt pin /IRQ. Regardless of the setting of the corresponding enable bit in the interrupt register, the ZXTO flag in the interrupt status register (MASK) is always set to active 1 when the ZXTOUT register decrements to 0.

Table 40 ZXTO

0x3F	**STATUS**		
Position	**Interrupt Flag**	**Default Value**	**Description**
4	ZXTO	0	zero-crossing timeout

Table 40 ZXTOUT

Addr	**Name**	**Bit Width**	**Default Value**	**Description**
8E	ZXTOUT	16	0xFFFF	If no zero-crossing signal is detected within the duration specified by this register, a zero-crossing timeout interrupt will be generated. Default value is FFFFH.

The zero-crossing timeout register ZXTOUT supports both read and write operations by users, with a default value of 0xFFFF. The register has a resolution of 64μs/LSB, thereby limiting the maximum interrupt delay time to 4.26 seconds.

The following diagram illustrates the zero-crossing timeout detection mechanism when the line voltage remains at a fixed DC signal level:

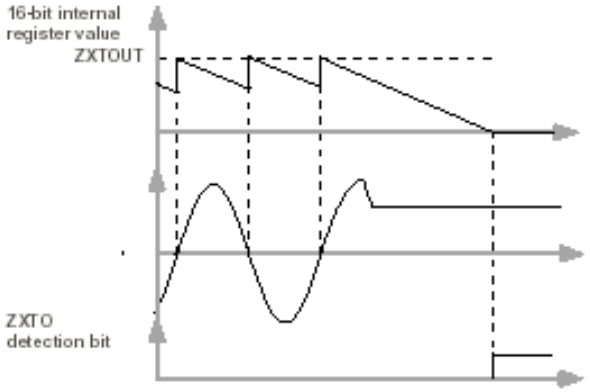


Figure 10 Zero-Crossing Timeout

7.1.7.5 Power Supply Monitoring

The chip integrates an on-board power monitoring circuit that continuously monitors the analog supply voltage (VDD). If the supply voltage falls below 2.7V ± 5%, the entire circuit remains deactivated (non-operational), meaning no energy accumulation is performed when VDD < 2.7V. This design ensures correct operation during power-up/power-down events.

The power monitoring circuit incorporates hysteresis and filtering mechanisms to significantly suppress false triggering caused by noise. Under normal conditions, the power supply decoupling network should maintain VDD ripple within 3.3V ±5%.

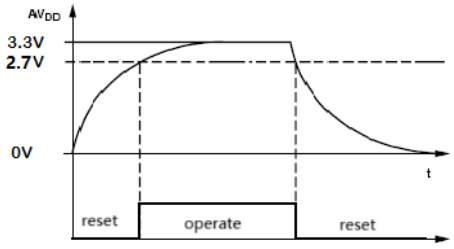


Figure 11 Power Supply Monitoring

7.2. Internal Registers

7.2.1 Electrical Parameter Registers (Read-Only)

Table 44 Electrical Parameter Registers

Addr	Name	Bit Width	Default Value	Description
1	IA_WAVE	24	0x000000	Current A waveform
2	IB_WAVE	24	0x000000	Current B waveform
3	V_WAVE	24	0x000000	Voltage waveform
4	IA_WAVE_DC	24	0x000000	Current A DC waveform
5	IB_WAVE_DC	24	0x000000	Current B DC waveform
6	V_WAVE_DC	24	0x000000	Voltage DC waveform
7	IA_RMS	24	0x000000	RMS of Current A
8	IB_RMS	24	0x000000	RMS of Current B
9	V_RMS	24	0x000000	RMS of Voltage
A	IA_FAST_RMS	24	0x000000	Fast RMS of Current A
B	IB_FAST_RMS	24	0x000000	Fast RMS of Current B
C	V_FAST_RMS	24	0x000000	Fast RMS of Voltage
10	A_WATT	24	0x000000	Active power (channel A), signed
11	B_WATT	24	0x000000	Active power (channel B), signed
12	A_VAR	24	0x000000	Reactive power (fundamental, A), signed
13	B_VAR	24	0x000000	Reactive power (fundamental, B), signed
14	A_WATT_DC	24	0x000000	DC power (channel A)
15	B_WATT_DC	24	0x000000	DC power (channel B)
16	A_VA	24	0x000000	Apparent power (channel A)
17	B_VA	24	0x000000	Apparent power (channel B)
18	A_WATT_SUM	24	0x000000	Total active power (AC + DC, channel A), signed

19	B_WATT_SUM	24	0x000000	Total active power (AC + DC, channel B), signed
1A	A_PF	24	0x000000	Power factor (channel A), signed
1B	B_PF	24	0x000000	Power factor (channel B), signed
1C	A_WATTHR	24	0x000000	Active energy (channel A)
1D	B_WATTHR	24	0x000000	Active energy (channel B)
1E	A_VARHR	24	0x000000	Reactive energy (fundamental, A)
1F	B_VARHR	24	0x000000	Reactive energy (fundamental, B)
20	A_DCHR	24	0x000000	DC energy (channel A)
21	B_DCHR	24	0x000000	DC energy (channel B)
22	A_VAHR	24	0x000000	Apparent energy (channel A), unsigned (optional)
23	B_VAHR	24	0x000000	Apparent energy (channel B), unsigned (optional)
24	A_SUMHR	24	0x000000	Total active energy (channel A)
25	B_SUMHR	24	0x000000	Total active energy (channel B)
26	A_CF_CNT	24	0x000000	Active pulse count (channel A)
27	B_CF_CNT	24	0x000000	Active pulse count (channel B)
28	A_CFQ_CNT	24	0x000000	Reactive pulse count (fundamental, A)
29	B_CFQ_CNT	24	0x000000	Reactive pulse count (fundamental, B)
2A	A_CF_DC_CNT	24	0x000000	DC power pulse count (channel A)
2B	B_CF_DC_CNT	24	0x000000	DC power pulse count (channel B)
2C	A_CFS_CNT	24	0x000000	Apparent pulse count (channel A, optional)
2D	B_CFS_CNT	24	0x000000	Apparent pulse count (channel B, optional)
2E	A_CF_SUM_CNT	24	0x000000	Total active pulse count (channel A)
2F	B_CF_SUM_CNT	24	0x000000	Total active pulse count (channel B)
30	SIGN	10	0x0000	Power sign register

31	IA_PK	24	0x000000	Peak value of current A waveform
32	IB_PK	24	0x000000	Peak value of current B waveform
33	V_PK	24	0x000000	Peak value of voltage waveform
35	PERIOD	20	0x00000	Line voltage frequency period
36	A_CORNER	16	0x0000	Phase angle between voltage and current (A)
37	B_CORNER	16	0x0000	Phase angle between voltage and current (B)
39	IA_FAST_RMS_HOLD	24	0x000000	Fast RMS of current A (held)
3A	IB_FAST_RMS_HOLD	24	0x000000	Fast RMS of current B (held)
3B	V_FAST_RMS_HOLD	24	0x000000	Fast RMS of voltage (held)
3C	Reserved	10	0x000000	NC
3D	Reserved	10	0x000000	NC
3E	STATUS_MF	3	0x00	MF status, unsigned
3F	STATUS	16	0x000000	Interrupt status, unsigned

7.2.2 User Operation Registers

Table 45 User Operation Registers

Addr	Name	Bit Width	Default Value	Description
40	USR_WRPROT	16	0x0000	User write protection setting. Writing **0x5555** enables operation of user registers from reg41 to regA8 and regC4.
41	SOFT_RESET	16	0x0000	System reset. Writing **0x5A5A** resets only the digital state machines and registers (Checksum calculation). Writing **0xAA55** resets user R/W registers: reg40 to regA8, regC0 to regCD (except regC6).
43	MODE_OUT	15	0x0000	Logic Output selection.
44	MODE	16	0x0000	User mode selection.

46	MASK	16	0x0000	Interrupt mask. Controls whether an interrupt generates a valid IRQ output. See "Interrupt Mask Register" description.
47	RST_CF_CNT	10	0x0000	Pulse count reset setting.
48	RST_ENG	10	0x0000	Energy reset setting. See "Read-with-Reset Configuration Register" description for details.
49	ADC_PD<3:0>	3	0x0	ADC channel enable control: [0] Voltage channel; [1] Current A channel; [2] Current B channel.

7.2.3 Calibration Registers

Table 46 Calibration Registers

Addr	Name	Bit Width	Default Value	Description
51	GAIN	12	0x000	Channel PGA gain adjustment. 0000=1, 0001=2, 0010=8, 0011=16, 0110=24, 0111=32. [11:8]: Current A channel, [7:4]: Current B channel, [3:0]: Voltage channel.
52	IRMS_P1	16	0x0100	Breakpoint P1 definition for angular error segmentation. Satisfies IRMSmin < P1 < P2 < IRMSmax.
53	IRMS_P2	16	0x2000	Breakpoint P2 definition for angular error segmentation. Satisfies IRMSmin < P1 < P2 < IRMSmax.
54	IA_PHCAL1	16	0x0000	Current A channel phase error calibration 1. When IRMSmin < Input RMS Current < P1 * 256, [6:0] is used for current channel phase correction. When P1 * 256 < Input RMS Current < P2 * 256, [14:8] is used for current channel phase correction. Adjustment accuracy same as above.
55	IA_PHCAL2	8	0x00	Current A channel phase error calibration 2. When P2 * 256 < Input RMS Current < IRMSmax, [6:0] is used for current channel phase correction.
56	IB_PHCAL1	16	0x0000	Current B channel phase error calibration 1 (Same as reg 54).
57	IB_PHCAL2	8	0x00	Current B channel phase error calibration 2 (Same as reg

				55).
58	V_PHCAL	8	0x00	Voltage channel phase error calibration (Same as reg 54).
5A	IA_CHOS	16	0x0000	Current A channel offset adjustment, two's complement.
5B	IB_CHOS	16	0x0000	Current B channel offset adjustment, two's complement.
5C	V_CHOS	16	0x0000	Voltage channel offset adjustment, two's complement.
5D	IA_CHOS_1	16	0x0000	Current A channel offset adjustment, two's complement.
5E	IB_CHOS_1	16	0x0000	Current B channel offset adjustment, two's complement.
5F	V_CHOS_1	16	0x0000	Voltage channel offset adjustment, two's complement.
60	IA_CHOS_8	16	0x0000	Current A channel offset adjustment, two's complement.
61	IB_CHOS_8	16	0x0000	Current B channel offset adjustment, two's complement.
62	V_CHOS_8	16	0x0000	Voltage channel offset adjustment, two's complement.
63	IA_CHOS_16	16	0x0000	Current A channel offset adjustment, two's complement.
64	IB_CHOS_16	16	0x0000	Current B channel offset adjustment, two's complement.
65	V_CHOS_16	16	0x0000	Voltage channel offset adjustment, two's complement.
66	IA_CHOS_32	16	0x0000	Current A channel offset adjustment, two's complement.
67	IB_CHOS_32	16	0x0000	Current B channel offset adjustment, two's complement.
68	V_CHOS_32	16	0x0000	Voltage channel offset adjustment, two's complement.
69	IA_CHGN	16	0x0000	Current A channel gain adjustment, two's complement.
6A	IB_CHGN	16	0x0000	Current B channel gain adjustment, two's complement.
6B	V_CHGN	16	0x0000	Voltage channel gain adjustment, two's complement.
6C	IA_RMSOS	16	0x0000	Current A RMS offset correction register.
6D	I B_RMSOS	16	0x0000	Current B RMS offset correction register.
6E	V_RMSOS	16	0x0000	Voltage RMS offset correction register.
71	IA_RMSGN	16	0x0000	Current A RMS gain adjustment.

72	IB_RMSGN	16	0x0000	Current B RMS gain adjustment.
73	V_RMSGN	16	0x0000	Voltage RMS gain adjustment.
74	A_WATTOS	16	0x0000	Channel A active power offset adjustment, two's complement.
75	B_WATTOS	16	0x0000	Channel B active power offset adjustment, two's complement.
76	A_WATTGN	16	0x0000	Channel A active power gain adjustment, two's complement.
77	B_WATTGN	16	0x0000	Channel B active power gain adjustment, two's complement.
78	A_WATTOS_DC	16	0x0000	Channel A DC active power offset adjustment, two's complement.
79	B_WATTOS_DC	16	0x0000	Channel B DC active power offset adjustment, two's complement.
7A	A_WATTGN_DC	16	0x0000	Channel A DC active power gain adjustment, two's complement.
7B	B_WATTGN_DC	16	0x0000	Channel B DC active power gain adjustment, two's complement.
7C	A_VAROS	16	0x0000	Channel A reactive power offset adjustment, two's complement.
7D	B_VAROS	16	0x0000	Channel B reactive power offset adjustment, two's complement.
7E	A_VARGN	16	0x0000	Channel A reactive power gain adjustment, two's complement.
7F	B_VARGN	16	0x0000	Channel B reactive power gain adjustment, two's complement.
80	A_VAOS	16	0x0000	Channel A apparent power offset adjustment, two's complement.
81	B_VAOS	16	0x0000	Channel B apparent power offset adjustment, two's complement.

82	A_VAGN	16	0x0000	Channel A apparent power gain adjustment, two's complement.
83	B_VAGN	16	0x0000	Channel B apparent power gain adjustment, two's complement.
84	A_WA_LOS	12	0x000	Channel A active power small signal compensation register, two's complement.
85	B_WA_LOS	12	0x000	Channel B active power small signal compensation register, two's complement.
86	A_VAR_LOS	12	0x000	Channel A reactive power small signal compensation register, two's complement.
87	B_VAR_LOS	12	0x000	Channel B reactive power small signal compensation register, two's complement.
88	WA_CREEP	12	0x04C	Active anti-creep power threshold (WA_CREEP).
89	VAR_CREEP	12	0x04C	Reactive anti-creep power threshold (VAR_CREEP).
8A	RMS_CREEP	12	0x200	RMS small signal threshold.
8B	REVP_CREEP	12	0x04C	Reverse power indication threshold.
8C	V_PKLVL	16	0xFFFF	Voltage peak threshold. [15:12]: Number of consecutive half-cycles for detection, [11:0]: High 12 bits of the detection threshold.
8D	I_PKLVL	16	0xFFFF	Current peak threshold. [15:12]: Number of consecutive half-cycles for detection, [11:0]: High 12 bits of the detection threshold.
8E	ZXTOUT	16	0xFFFF	Zero-crossing timeout. If no zero-crossing signal is detected within the time specified by this register, a zero-crossing timeout interrupt will be generated. Default is FFFFH.
91	SAGCYC	8	0x04	Sag line cycle count. Default is 04H.
92	SAGLVL	12	0x100	Sag voltage threshold. If the voltage channel input remains continuously below this register value for longer than the time in SAGCYC, a line voltage sag interrupt will be generated. Default 100H (~1/16 full-scale voltage

				input).
93		13	0x0FFF	Reserved, participates in checksum.
94	IA_FAST_RMS_CTRL1	12	0x20F	[11:9]: Current A channel fast RMS register refresh time (options: half-cycle or N cycles, default: cycle); [8:0]: High 9 bits [20:12] of the channel fast RMS threshold register.
95	IA_FAST_RMS_CTRL2	12	0xFFF	Current A channel fast RMS threshold register low 12 bits [11:0].
96	IB_FAST_RMS_CTRL1	12	0x20F	[11:9]: Current B channel fast RMS register refresh time (options: half-cycle or N cycles, default: cycle); [8:0]: High 9 bits [20:12] of the channel fast RMS threshold register.
97	IB_FAST_RMS_CTRL2	12	0xFFF	Current B channel fast RMS threshold register low 12 bits [11:0].
98	V_FAST_RMS_CTRL1	12	0x20F	[11:9]: Voltage channel fast RMS register refresh time (options: half-cycle or N cycles, default: cycle); [8:0]: High 9 bits [20:12] of the channel fast RMS threshold register.
99	V_FAST_RMS_CTRL2	12	0xFFF	Voltage channel fast RMS threshold register low 12 bits [11:0].
9A	flag_ctrl	12	0x0	[11:9]: Master control selection for M3-M1: 0=Output internal indication; 1=Master direct control. [8:6]: Master direct control level state for M3~M1 outputs. [5:3]: Indication selection for M3-M1: 0=Output real-time interrupt; 1=Output delayed control. [2:0]: Delay control for M3-M1=0: 0=Disable, 1=Enable.
9B	flag_ctrl1	16	0x0000	Overcurrent indication control register 1. Trip delay timer (0.1ms/lsb).
9C	flag_ctrl2	16	0x0000	Overcurrent indication control register 2. Close delay timer (0.1ms/lsb).
9D	Reserved	16	0x07FF	Reserved.
9E	Reserved	12	0x000	Reserved.

9F	Reserved	12	0x000	Reserved.
A0	VAR_PHCAL_B	16	0x0000	Reactive power angle correction (B).
A1	VAR_PHCAL_A	16	0x0000	Reactive power angle correction (A).
A2	CFDIV	12	0x010	Active power CF scaling register.
A3	ZXVLVL	16	0x0001	
A4	ZXILVL	16	0x0001	
A5	RESERVE1	8	0x00	
A6	OTP checksum1	16	0x2100	OTP register checksum (checksum1). If error, revert to default value. Covers reg51 to reg6E, plus RegC5.
A7	OTP checksum2	16	0x02E1	OTP register checksum (checksum2). If error, revert to default value. Covers reg71 to reg8E, plus RegC5.
A8	OTP checksum3	16	0x3F38	OTP register checksum (checksum3). If error, revert to default value. Covers reg91 to regA5, plus RegC5.

7.2.4 Detailed Description of Electrical Parameter Registers

7.2.4.1 Waveform Registers

Table 47 Waveform Registers

Addr	Name	Bit Width	Default Value	Description
1	IA_WAVE	24	0x000000	Current A Waveform
2	IB_WAVE	24	0x000000	Current B Waveform
3	V_WAVE	24	0x000000	Voltage Waveform
4	IA_WAVE_DC	24	0x000000	Current A DC Waveform
5	IB_WAVE_DC	24	0x000000	Current B DC Waveform
6	V_WAVE_DC	24	0x000000	Voltage DC Waveform

Waveform data of real-time sampling points. Sampling rate: 20ms/64 = 312.5 samples per cycle, approximately 312 samples per cycle.

7.2.4.2 RMS (Root Mean Square) Registers

Table 48 RMS Registers

Addr	Name	Bit Width	Default Value	Description
7	IA_RMS	24	0x000000	Current A RMS Value
8	IB_RMS	24	0x000000	Current B RMS Value
9	V_RMS	24	0x000000	Voltage RMS Value
A	IA_FAST_RMS	24	0x000000	Current A Fast RMS Value
B	IB_FAST_RMS	24	0x000000	Current B Fast RMS Value
C	V_FAST_RMS	24	0x000000	Voltage Fast RMS Value

Conversion Formula Between Register Values and Input Signals (Typical Values)

Current RMS Register: I_RMS = $\frac{6923*V(A)*GAIN\_I}{Vref}$

Voltage RMS Register: V_RMS = $\frac{6704*V(V)*GAIN\_V}{Vref}$

Where:

- *V*(*A*): Voltage signal at current input pin (unit: mV)
- *V*(*V*): Voltage signal at voltage input pin (unit: mV)
- *Vref*: Reference voltage (typical value: 1.0975V)
- *GAINI*, *GAINV*: Gain factors for current and voltage channels, respectively

The fast RMS and RMS values are calculated using different algorithms, with the following scaling relationship:

$$FAST\_RMS \approx RMS * 0.55$$

7.2.4.3 Active Power Registers

Table 49 Active Power Registers

Addr	Name	Bit Width	Default Value	Description
10	A_WATT	24	0x000000	Channel A Active Power (Signed)
11	B_WATT	24	0x000000	Channel B Active Power (Signed)

The active power registers store signed 24-bit data in two's complement format.

The MSB (Bit[23]) serves as the sign bit: Bit[23]=1 indicates negative power (reverse power flow).

Power Calculation Formula:

$$WATT = \frac{11.073*V(A)*GAIN\_I*V(V)*GAIN\_V*Cos(\emptyset)}{Vref^2}$$

Parameter Definitions:

- *V*(*A*): Voltage signal at current input pin (unit: mV)
- *V*(*V*): Voltage signal at voltage input pin (unit: mV)
- *Vref*: Reference voltage (typical value: 1.0975V)
- *GAINI*, *GAINV*: Gain factors for current and voltage channels respectively
- cos(*ϕ*): Power factor (phase angle between voltage and current)

7.2.4.4 Reactive Power Registers

Table 50 Reactive Power Registers

Addr	Name	Bit Width	Default Value	Description
12	A_VAR	24	0x000000	Channel A (fundamental) reactive power, signed
13	B_VAR	24	0x000000	Channel B (fundamental) reactive power, signed

7.2.4.5 DC Power Registers

Table 51 DC Power Registers

Addr	Name	Bit Width	Default Value	Description
14	A_WATTDC	24	0x000000	Channel A DC power
15	B_WATTDC	24	0x000000	Channel B DC power

7.2.4.6 Apparent Power Registers

Table 52 Apparent Power Registers

Addr	Name	Bit Width	Default Value	Description
16	A_VA	24	0x000000	Channel A apparent power
17	B_VA	24	0x000000	Channel B apparent power

7.2.4.7 Power Factor Registers

Table 53 Power Factor Registers

Addr	Name	Bit Width	Default Value	Description
1A	A_PF	24	0x000000	Channel A power factor register
1B	B_PF	24	0x000000	Channel B power factor register

24-bit signed number in two's complement. Bit[23] is the sign bit.

$$\text{Power factor} = \frac{PF}{2^{23}}$$

7.2.4.8 Energy Registers

Table 54 Energy Registers

Addr	Name	Bit Width	Default Value	Description
1C	A_WATTHR	24	0x000000	Active energy of Channel A
1D	B_WATTHR	24	0x000000	Active energy of Channel B
1E	A_VARHR	24	0x000000	Reactive (fundamental) energy of Channel A
1F	B_VARHR	24	0x000000	Reactive (fundamental) energy of Channel B
20	A_DCHR	24	0x000000	DC energy of Channel A
21	B_DCHR	24	0x000000	DC energy of Channel B
22	A_VAHR	24	0x000000	Apparent energy of Channel A, unsigned (optional)
23	B_VAHR	24	0x000000	Apparent energy of Channel B, unsigned (optional)
24	A_SUMHR	24	0x000000	Total active energy of Channel A
25	B_SUMHR	24	0x000000	Total active energy of Channel B

7.2.4.9 Energy Pulse Count Registers

Table 55 Energy Pulse Count Registers

Addr	Name	Bit Width	Default Value	Description
26	A_CF_CNT	24	0x000000	Active pulse count for Channel A
27	B_CF_CNT	24	0x000000	Active pulse count for Channel B
28	A_CFQ_CNT	24	0x000000	Reactive (fundamental) pulse count for Channel A

29	B_CFQ_CNT	24	0x000000	Reactive (fundamental) pulse count for Channel B
2A	A_CF_DC_CNT	24	0x000000	DC power pulse count for Channel A
2B	B_CF_DC_CNT	24	0x000000	DC power pulse count for Channel B
2C	A_CFS_CNT	24	0x000000	Apparent pulse count for Channel A (optional)
2D	B_CFS_CNT	24	0x000000	Apparent pulse count for Channel B (optional)
2E	A_CF_SUM_CNT	24	0x000000	Total active pulse count for Channel A
2F	B_CF_SUM_CNT	24	0x000000	Total active pulse count for Channel B

7.2.4.10 Power Sign Bit Register

Table 56 Power Sign Bit Register

Addr	Name	Bit Width	Default Value	Description
30	SIGN	10	0x0000	Power sign bit register

7.2.4.11 Peak Registers

Table 57 Peak Registers

Addr	Name	Bit Width	Default Value	Description
31	IA_PK	24	0x000000	Current A waveform peak register
32	IB_PK	24	0x000000	Current B waveform peak register
33	V_PK	24	0x000000	Voltage waveform peak register

7.2.4.12 Line Voltage Frequency Register

Table 58 Line Voltage Frequency Register

Addr	Name	Bit Width	Default Value	Description
35	PERIOD	20	0x000000	Line voltage period register

Measures the frequency of the sine wave signal from the selected voltage channel.

$$\text{Line voltage frequency} = \frac{10000000}{PERIOD}\ \text{Hz}$$

7.2.4.13 Voltage-Current Phase Angle Registers

Table 59 Voltage-Current Phase Angle Registers

Addr	Name	Bit Width	Default Value	Description
36	A_CORNER	16	0x000000	Phase angle register between voltage and current waveforms in Channel A
37	B_CORNER	16	0x000000	Phase angle register between voltage and current waveforms in Channel B

Note: The phase angle registers will not be updated when current falls below a specified threshold.

$$\text{Phase angle (deg)} = \frac{360 * ANGLE[N] * f_c}{500000}$$

where fc is the measured frequency of the AC signal source, typically 50 Hz.

7.2.4.14 Status Registers

Table 60 Status Registers

Addr	Name	Bit Width	Default Value	Description
3E	STATUS_MF	3	0x00	MF status (unsigned)
3F	STATUS	16	0x000000	Interrupt status (unsigned)

7.2.5 Detailed Description of User Operation Registers

7.2.5.1 User Write Protection Setting Register

Table 61 User Write Protection Setting Register

Addr	Name	Bit Width	Default Value	Description
40	USR_WRPROT	16	0x0000	User write protection setting register. Writing 0x5555 enables operations on user registers (reg41 to regA8, regC4).

The BL0973 implements a strict register write protection mechanism. To modify other registers, 0x5555 must first be written to the write protection setting register.

7.2.5.2 Soft Reset Register

Table 62 Soft Reset Register

Addr	Name	Bit Width	Default Value	Description
41	SOFT_RESET	16	0x000000	When input is 5A5A5A, system resets—only resets digital state machine and registers! When input is 55AA55, user read/write register reset—Reset: reg40 to regA8, regC0 to regCD (except regC6).

7.2.5.3 Output Mode Register

Table 63 Output Mode Register

0x43	MODE_OUT	Output Mode Register	
No.	**name**	**default value**	**description**
[3:0]	MF1_SEL	4'b0000	MF1 pin output configuration
[7:4]	CF_SEL	4'b0000	CF pulse output configuration (10 options available): 0000 - CF disabled; 0001 - A_CF; 0010 - B_CF; 0011 - A_CFQ; 0100 - B_CFQ; 0101 - A_CF_DC; 0110 - B_CF_DC; 0111 - A_CFS; 1000 - B_CFS; 1001 - A_CF_SUM; 1010 - B_CF_SUM
[10:8]	AVG_SEL	3'b000	Fast RMS register output selection: Default 0 selects fast RMS, 1 selects DC average
[14:11]	MF2_SEL	4'b0000	MF2 pin output configuration
[15]	mode_all	1'b0	Mode selection: 1 - 3I (three-current mode); 0 - 1U2I (one-voltage two-current mode, default)

Table 64 MFx configuration

MFx_SEL[3:0]	MF1 [3:0]	MF2 [14:11]
0000	MF1	MF2
0001	ZX_V	ZX_V
0010	ZX_IA	ZX_IA

0011	ZX_IB	ZX_IB
0100	nSAG	nSAG
0101	ZXTO	ZXTO
0110	PK_IA	PK_IA
0111	PK_IB	PK_IB
1000	PK_V	PK_V
1001	REVPAP_A	REVPAP_A
1010	REVPAP_B	REVPAP_B
1011	REVPRP_A	REVPRP_A
1100	REVPRP_B	REVPRP_B
1101	VREF_LOW	VREF_LOW
1110	INPUT_CKS_ERR	INPUT_CKS_ERR
1111	MF2	MF1

7.2.5.4 User Mode Selection Register

Table 65 User Mode Selection Register

0x44	**MODE**	**Operation Mode Register**	
No.	**name**	**default value**	**description**
[0]	L_F_SEL	1'b0	Fast RMS selection with high-pass filter (HPF): 0 - No HPF (default); 1 - With HPF
[3:1]	WAVE_SEL	3{1'b0}	Active power waveform selection: 0 - With HPF; 1 - Without HPF
[9:4]	WAVE_RMS_SEL	3{2'b00}	RMS waveform selection: 11 - HPF; 10 - DC; 01 - Post-sinc; 00 - HPF • [9:8] Voltage • [7:6] Current B • [5:4] Current A

[10]	WAVE_REG_SEL	1'b0	Current WAVE register output selection: 0 - Normal current channel waveform (default); 1 - Fast RMS measurement channel waveform
[11]	CF_ADD_SEL	1'b0	Watt/Var energy accumulation method: 0 - Absolute sum; 1 - Algebraic sum
[12]	VA_SEL	1'b0	VA algorithm selection: 0 - rmsi*rmsv； 1 - (watt^2+var^2)^0.5
[14:13]	RMS_UPDATE_SEL	2'b00	RMS register update rate: 11-1000ms, 00-500ms(default), 01-250ms; 10-125ms
[15]	AC_FREQ_SEL	1'b0	AC frequency selection: 1 - 60Hz; 0 - 50Hz (default)

7.2.5.5 Interrupt Mask Register

Table 66 Interrupt Mask Register

Bit Position	Interrupt Flag	Default Value	Description
0	ZX03	0	Indicates voltage waveform zero-crossing (sign bit detected)
1	ZX01	0	Indicates current A waveform zero-crossing (sign bit detected)
2	ZX02	0	Indicates current B waveform zero-crossing (sign bit detected)
3	SAG	0	Voltage sag interrupt: 1 = sag detected
4	ZXTO	0	Zero-crossing timeout interrupt: 1 = timeout occurred
5	PK_IA	0	Current A RMS peak exceeds PKILVL threshold: 1 = interrupt triggered
6	PK_IB	0	Current B RMS peak exceeds PKILVL threshold: 1 = interrupt triggered
7	PK_V	0	Voltage RMS peak exceeds PKVLVL threshold: 1 = interrupt triggered
8	REVPAP_A	0	Sign reversal detected in active power calculation (Phase A)
9	REVPAP_B	0	Sign reversal detected in active power calculation (Phase B)

10	REVPRP_A	0	Sign reversal detected in reactive power calculation (Phase A)
11	REVPRP_B	0	Sign reversal detected in reactive power calculation (Phase B)
12	VREF_LOW	0	Reference voltage low: 1 = VREF < 1V; 0 = normal
13	INPUT_CKS_ERR	0	Input checksum error: 1 = checksum mismatch
14			
15			

7.2.5.6 Read-with-Reset Configuration Register

Table 67 Read-with-Reset Configuration Register

Addr	Name	Bit Width	Default Value	Description
47	RST_CF_CNT	10	0x000	Configures read-with-reset behavior for energy pulse counter registers
48	RST_ENG	10	0x000	Configures read-with-reset behavior for energy accumulation registers

When Bit[9:0] is set to 1, the corresponding energy-related register will clear automatically after being read. Each bit can be configured independently.

Table 68 energy-related register configuration

Bit[9:0]	9	8	…	2	1	0
Energy Registers (0x_)	25	24	…	1E	1D	1C
Pulse Registers (0x_)	2F	2E	…	28	27	26

7.2.5.7 ADC Enable Control

Table 69 ADC Enable Control

Addr	Name	Bit Width	Default Value	Description
49	ADC_PD	3	0x0	Controls enable/disable for 3 analog channel ADCs: [0]- Voltage channel； [1]- Current A channel；[2]- Current B channel

To reduce power consumption, disable unused ADC channels by setting their corresponding bits to 1.

7.2.6 Calibration Register Details

7.2.6.1 PGA Channel Gain Adjustment

Table 70 PGA Channel Gain Adjustment Register

Addr	Name	Bit Width	Default Value	Description
51	GAIN	12	0x000	PGA channel gain adjustment register. [3:0]: Voltage channel； [7:4]: Current B channel; [11:8]: Current A channel

Each 4-bit controls one channel: [0010]=8x; [0011]=16x; [0110]=24x; [0111]=32x;

After PGA gain setting, the maximum allowable input signal for the channel needs to be reduced accordingly.

Table 71 PGA Gain and Maximum Allowable Input Signal

GAIN[3:0]	PGA Gain Factor	Maximum Allowable Input Signal (Typical)
0010	8	Differential Voltage 175mV
0011	16	Differential Voltage 87.5mV
0110	24	Differential Voltage 58.3mV
0111	32	Differential Voltage 43.75mV (31mV rms)

Note: To reduce crosstalk between analog channels, the PGA gain settings for current and voltage channels can be selected from 16x, 24x, or 32x gain factors.

7.2.6.2 Phase Correction Related Registers

Table 72 Current Channel Angle Error Segment Definition Registers

Addr	Name	Bit Width	Default Value	Description
52	IRMS_P1	16	0x0100	Angle error segment point P1, must satisfy IRMSmin<P1*256<P2*256<IRMSmax
53	IRMS_P2	16	0x2000	Angle error segment point P2, must satisfy IRMSmin<P1*256<P2*256<IRMSmax

Current transformers may exhibit different angle errors at varying current levels. The BL0973 supports segmented phase compensation based on RMS current values.

Table 73 Error Correction

Addr	Name	Bit Width	Default Value	Description
54	IA_PHCAL1	16	0x0000	Current Channel A Angle Error Correction 1: When IRMSmin < input RMS current < P1 * 256, [6:0] is used for current channel phase correction. When P1 * 256 < input RMS current < P2 * 256, [14:8] is used for current channel phase correction (adjustment precision same as above).
55	IA_PHCAL2	8	0x00	Current Channel A Angle Error Correction 2: When P2 * 256 < input RMS current < IRMSmax, [6:0] is used for current channel phase correction.
56	IB_PHCAL1	16	0x0000	Current Channel B Angle Error Correction 1 (Same as Register 53)
57	IB_PHCAL2	8	0x00	Current Channel B Angle Error Correction 2 (Same as Register 54)
58	V_PHCAL	8	0x00	Voltage Channel Angle Error Correction (Same as Register 53)
A0	VAR_PHCAL_B	16	0x0000	Reactive Power Angle Compensation
A1	VAR_PHCAL_A	16	0x0000	Reactive Power Angle Compensation

Taking the current channel A angle error correction register as an example:

When IRMSmin < input RMS current (IA_RMS) < P1 * 256:

IA_PHCAL1[7:0] is used for current channel phase correction

Minimum adjustment step: 250ns (corresponding to 0.0045°/LSB)

Maximum adjustable range: ±0.574°

When P1 * 256 < IA_RMS < P2 * 256:

IA_PHCAL[15:8] is used for phase correction with same precision as above

When P2 * 256 < IA_RMS < IRMSmax:

IA_PHCAL[23:16] is used for phase correction with same precision

(Minimum adjustment step: 250ns ↔ 0.0045°/LSB; Corresponding error ≈ 1.732*Sin(0.0045°) = 0.0136%; Maximum adjustment range ≈ 0.574°; Maximum adjustment error ≈ 1.734%)

7.2.6.3 Channel Offset Adjustment

Table 74 Channel Offset Adjustment Register

Addr	Name	Bit Width	Default Value	Description
5A	IA_CHOS	16	0x0000	Current Channel A Offset Adjustment Register, two's complement
5B	IB_CHOS	16	0x0000	Current Channel B Offset Adjustment Register, two's complement
5C	V_CHOS	16	0x0000	Voltage Channel Offset Adjustment Register, two's complement
5D	IA_CHOS_1	16	0x0000	Current Channel A Offset Adjustment, two's complement
5E	IB_CHOS_1	16	0x0000	Current Channel B Offset Adjustment, two's complement
5F	V_CHOS_1	16	0x0000	Voltage Channel Offset Adjustment, two's complement
60	IA_CHOS_8	16	0x0000	Current Channel A Offset Adjustment, two's complement
61	IB_CHOS_8	16	0x0000	Current Channel B Offset Adjustment, two's complement
62	V_CHOS_8	16	0x0000	Voltage Channel Offset Adjustment, two's complement
63	IA_CHOS_16	16	0x0000	Current Channel A Offset Adjustment, two's complement
64	IB_CHOS_16	16	0x0000	Current Channel B Offset Adjustment, two's complement
65	V_CHOS_16	16	0x0000	Voltage Channel Offset Adjustment, two's complement
66	IA_CHOS_32	16	0x0000	Current Channel A Offset Adjustment, two's complement
67	IB_CHOS_32	16	0x0000	Current Channel B Offset Adjustment, two's complement
68	V_CHOS_32	16	0x0000	Voltage Channel Offset Adjustment, two's complement

The data in two's complement format is used to eliminate the offset introduced by the analog-to-digital conversion in current and voltage channels, respectively. This offset may originate from the input or the inherent offset of the ADC circuit itself. Offset correction ensures that the waveform offset is zero under no-load conditions.

$$\mathrm{WAVE[N]} = \mathrm{WAVE0[N]} + \mathrm{CHOS[N]}$$

where WAVE0[N] is the measured value of the corresponding channel, CHOS[N] is the offset calibration value of the corresponding channel and WAVE[N] is the calibrated output value.

7.2.6.4 Channel Gain Adjustment

Table 75 Channel Gain Adjustment Register

Addr	Name	Bit Width	Default Value	Description
69	IA_CHGN	16	0x0000	Current Channel A Gain Adjustment Register, two's complement
6A	IB_CHGN	16	0x0000	Current Channel B Gain Adjustment Register, two's complement
6B	V_CHGN	16	0x0000	Voltage Channel Gain Adjustment Register, two's complement

A 16-bit signed number in two's complement format is used to adjust the gain of the ADC sampling waveform for the corresponding channel, with an adjustable range of ±50%.

$$X\_WAVE = X\_WAVE0 * (1 + \frac{X\_CHGN}{2^{16}})$$

where X_WAVE0 is the measured value of the corresponding channel, X_CHGN is the gain adjustment value of the corresponding channel and X_WAVE is the calibrated output value.

7.2.6.5 RMS Offset Calibration

Table 76 RMS Offset Calibration Register

Addr	Name	Bit Width	Default Value	Description
6C	IA_RMSOS	16	0x0000	Current Channel A RMS Offset Calibration Register
6D	IB_RMSOS	16	0x0000	Current Channel B RMS Offset Calibration Register
6E	V_RMSOS	16	0x0000	Voltage Channel RMS Offset Calibration Register

Format: Two's complement with MSB as sign bit. Used to eliminate deviations in RMS calculations caused by input noise, ensuring RMS register values approach zero under no-load conditions.

$$X\_RMS = \sqrt{X\_RMS0^2 + X\_RMSOS * 256}$$

where X_RMS0 is measured RMS value of the corresponding channel, X_RMSOS is offset calibration value for the corresponding channel (two's complement format) and X_RMS is calibrated RMS output value.

7.2.6.6 RMS Gain Adjustment

Table 77 RMS Gain Adjustment Register

Addr	Name	Bit Width	Default Value	Description
71	IA_RMSGN	16	0x0000	Current Channel A RMS Gain Adjustment Register
72	IB_RMSGN	16	0x0000	Current Channel B RMS Gain Adjustment Register
73	V_RMSGN	16	0x0000	Voltage Channel RMS Gain Adjustment Register

Format: Two's complement with MSB as sign bit, providing ±50% adjustment range.

$$X\_RMS = X\_RMS0 * (1 + \frac{X\_RMSGN}{2^{16}})$$

where X_RMS0 is the RMS measurement value of the corresponding channel, X_RMSGN is the gain adjustment value of the corresponding channel, and X_RMS is the corresponding calibrated RMS output value.

7.2.6.7 Power Offset Calibration

Table 78 Power Offset Calibration Register

Addr	Name	Bit Width	Default Value	Description
74	A_WATTOS	16	0x0000	Channel A active power offset adjustment register, two's complement
75	B_WATTOS	16	0x0000	Channel B active power offset adjustment register, two's complement
78	A_WATTOS_DC	16	0x0000	Channel A DC active power offset adjustment, two's complement
79	B_WATTOS_DC	16	0x0000	Channel B DC active power offset adjustment, two's complement
7C	A_VAROS	16	0x0000	Channel A reactive power offset adjustment, two's complement
7D	B_VAROS	16	0x0000	Channel B reactive power offset adjustment, two's complement

80	A_VAOS	16	0x0000	Channel A apparent power offset adjustment, two's complement
81	B_VAOS	16	0x0000	Channel B apparent power offset adjustment, two's complement
84	A_WA_LOS	12	0x000	Channel A active power small signal compensation register, two's complement
85	B_WA_LOS	12	0x000	Channel B active power small signal compensation register, two's complement
86	A_VAR_LOS	12	0x000	Channel A reactive power small signal compensation register, two's complement
87	B_VAR_LOS	12	0x000	Channel B reactive power small signal compensation register, two's complement

Two's complement, with the most significant bit as the sign bit, is used to eliminate power deviation caused by board-level noise.

Taking active power offset correction as an example, the formula is as follows:

$$WATT[N] = WATT0[N] + \frac{WATTOS[N]}{2}$$

where WATT0[N] is the measured value of a specific channel, WATTOS[N] is the corresponding offset correction value (in two's complement) and WATT[N] is the calibrated output value.

The offset correction formulas for reactive power and apparent power are similar.

7.2.6.8 Power Gain Adjustment

Table 79 Power Gain Adjustment Register

Addr	Name	Bit Width	Default Value	Description
76	A_WATTGN	16	0x0000	Channel A active power gain adjustment, two's complement
77	B_WATTGN	16	0x0000	Channel B active power gain adjustment, two's complement
7A	A_WATTGN_DC	16	0x0000	Channel A DC active power gain adjustment, two's complement
7B	B_WATTGN_DC	16	0x0000	Channel B DC active power gain adjustment, two's complement

7E	A_VARGN	16	0x0000	Channel A reactive power gain adjustment, two's complement
7F	B_VARGN	16	0x0000	Channel B reactive power gain adjustment, two's complement
82	A_VAGN	16	0x0000	Channel A apparent power gain adjustment, two's complement
83	B_VAGN	16	0x0000	Channel B apparent power gain adjustment, two's complement

Taking active power gain adjustment as an example, the calculation is as follows:

$$\mathrm{WATT[N]} = \mathrm{WATT0[N]} * (1 + \frac{WATTGN[N]}{2^{16}})$$

Where WATT[N] represents the calibrated active power of channel N after adjustment, WATT0[N] represents the measured active power of channel N before adjustment and WATTGN[N] is the gain adjustment value (in two's complement format) for channel N.

The adjustment range is ±50%.

The gain correction formulas for reactive power and apparent power follow the same principle.

7.2.6.9 Anti-Creep Threshold Settings

Table 80 Anti-Creep Threshold Registers

Addr	Name	Bit Width	Default Value	Description
88	WA_CREEP	12	0x04C	Active power anti-creep threshold
89	VAR_CREEP	12	0x04C	Reactive power anti-creep threshold
8A	RMS_CREEP	12	0x200	RMS small signal threshold
8B	REVP_CREEP	12	0x04C	Reverse power indication threshold

To eliminate interference caused by noise signals, these registers can force the corresponding values to zero when no valid load signal is present.

Taking the active power anti-creep threshold (WA_CREEP) as an example:

When the absolute value of the input power signal is less than WA_CREEP × 2, the output power register value is set to zero. This ensures that under no-load conditions, even if small noise signals exist, the active power register output will remain 0.

The other threshold registers operate similarly.

7.2.6.10 CF Scaling Factor Configuration

Used to control the accumulation rate of energy pulse counting. The default setting for BL6552 is 0x10.

Table 81 CF Scaling Factor Register

Addr	Name	Bit Width	Default Value	Description
A2	CFDIV	12	0x010	CF Scaling Factor Register [11:0]

When CFDIV=0x10 is set as the reference frequency for energy pulse counting, the counting rate multipliers for other settings are as follows。

Table 82 Counting Multipliers

CFDIV	Counting Multiplier	CFDIV	Counting Multiplier
0x00	0.03125	0x40	4
0x01	0.0625	0x80	8
0x02	0.125	0x100	16
0x04	0.25	0x200	32
0x08	0.5	0x400	64
0x10	1	0x800	256
0x20	2	Other values	1

7.2.7 Fault Detection Configuration

Refer to Section 7.7 "Fault Detection" for detailed descriptions.

8. Application Information

8.1 Communication Interface

All register data is transmitted in 3-byte (24-bit) segments. If the register data is less than 3 bytes, unused bits are padded with 0s to complete the 3-byte transmission.

The communication mode is selected via the SEL pin: SPI mode when SEL=1, UART mode when SEL=0.

8.1.1 SPI

8.1.1.1 Overview

- Slave mode, 4-wire SPI, half-duplex communication, maximum communication rate < 750 K
- 8-bit data transmission, MSB first, LSB last
- Fixed clock polarity/phase (CPOL=0, CPHA=1)
- The device is selected when CS is pulled low.

8.1.1.2 Operating Mode

The master operates in Mode1: CPOL=0, CPHA=1. In idle state, SCLK remains at low level. Data

transmission occurs on the first edge, i.e., the transition of SCLK from low to high level. Thus, data sampling is performed on the falling edge, while data transmission occurs on the rising edge.

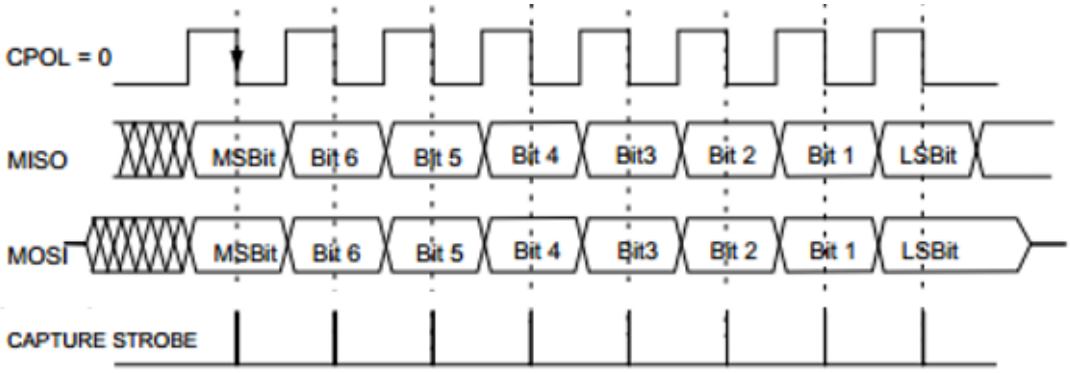


Figure 12 SPI

8.1.1.3 Frame Structure

In communication mode, an 8-bit identification byte (0x81 or 0x82) is sent first. (0x82) is the read identification byte, and (0x81) is the write identification byte. This is followed by the register address byte, which determines the address of the register to be accessed (refer to the BL0973 register list). The diagrams below illustrate the data transmission sequence for read and write operations, respectively. After completing a frame transmission, the BL0973 re-enters communication mode. Each read/write operation requires 48 SCLK pulses.

There are two types of frame structures, described as follows:

1) Write Register

Cmd: {0x81} + Addr + Data_H + Data_M + Data_L + SUM

{0x81} is the frame identification byte for write operations.

Addr is the internal register address of the BL0973 for the write operation.

The checksum byte (CHECKSUM) is calculated as (({0x81} + ADDR + DATA_H + DATA_M + DATA_L) & 0xFF), then bitwise inverted.

Write Operation Frame	0x81	ADDR[7:0]	DATA_H[7:0]	DATA_M[7:0]	DATA_L[7:0]	CHECKSUM[7:0]

Figure 13 SPI Write

2) Read Register

Cmd: {0x82} + Addr

Response: Data_H + Data_M + Data_L + SUM

{0x82} is the frame identification byte for read operations.

Addr is the internal register address of the BL0973 for the read operation.

The checksum byte (CHECKSUM) is calculated as (({0x82} + ADDR + DATA_H + DATA_M + DATA_L) & 0xFF), then bitwise inverted.

Read Command Frame	0x82	ADDR[7:0]	
Read Data Frame	DATA_H[7:0]	DATA_M[7:0]	DATA_L[7:0]	CHECKSUM[7:0]

Figure 14 SPI Read

8.1.1.4 Read Operation Timing

During data read operations on the BL0973, at the rising edge of SCLK, the BL0973 shifts out the corresponding data bit to the DOUT logic output pin. During the subsequent high period of SCLK, the DOUT value remains unchanged, allowing the external device to sample the DOUT value at the next falling edge. Similar to data write operations, the MCU must first send the identification byte and address byte before performing a data read operation.

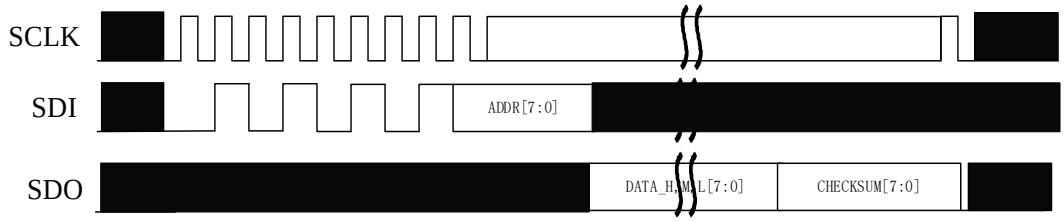


Figure 15 SPI Read Timing

When the BL0973 is in communication mode, the frame identification byte {0x82} indicates that the next data transfer operation is a read. This is immediately followed by the address byte of the target register to be read.

The BL0973 begins shifting out register data at the rising edge of SCLK. All remaining bits of the register data are subsequently shifted out at each following SCLK rising edge. Therefore, at the falling edge, external devices can sample the SPI output data.

Once the read operation is completed, the serial interface returns to communication mode. At this point, the DOUT logic output enters a high-impedance state at the falling edge of the last SCLK signal.

8.1.1.5 Write Operation Timing

The serial write sequence operates as follows:

The frame identification byte {0x81} indicates a write operation for data transfer. The MCU prepares the data bits to be written into the BL0973 before the falling edge of SCLK. At this falling edge, the register data begins to be shifted in.

All remaining bits of the register data are also shifted left (LSB first) at each subsequent SCLK falling edge.

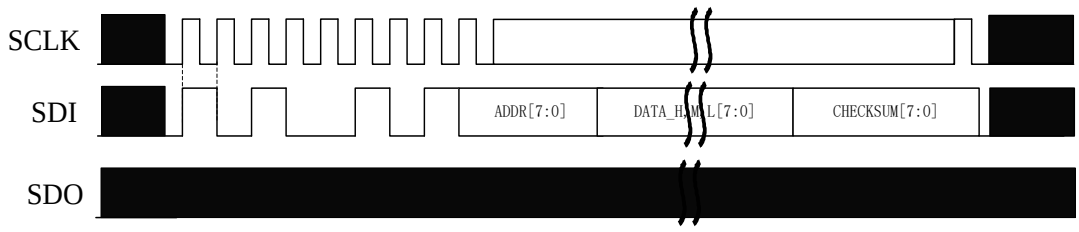


Figure 16 SPI Write Timing

SPI Interface Fault Tolerance Mechanism:

1) Frame Error Handling: If the frame identification byte or checksum (SUM) byte is incorrect, the entire frame data is discarded.
2) SPI Module Reset: The SPI interface can be individually reset by transmitting 6 consecutive bytes of 0xFF via the SPI interface.
3) CS Pull-Up Reset: Pulling the _CS signal high also triggers a reset of the interface.

8.1.2 UART

8.1.2.1 Overview

The communication mode is selected via the SEL pin: SPI mode when SEL=1, UART mode when SEL=0.

Configurable baud rates: 4800bps/9600bps/19200bps/38400bps, no parity, 1 stop bit.

Table 83 UART Baud Rate

Baud Rate Setting	4800	9600	19200	38400
CS Pin	0	0	1	1
SCLK Pin	0	1	0	1

In UART mode, the CS and SCLK pins serve as baud rate configuration pins.

The UART supports cascading functionality, allowing up to 16 BL0973 chips to be connected on the UART bus for time-division communication. The device address of the chip can be set via pins A4~A1, supporting 16 addresses from 0b0000 to 0b1111.

8.1.2.2 Byte Format

Taking 4800bps as an example:

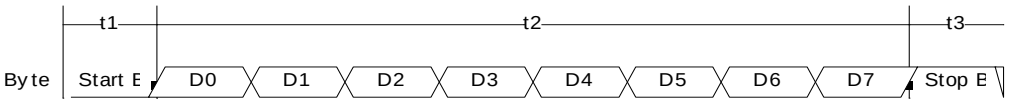


Figure 17 UART Byte Format

Start bit low-level duration: t1 = 208μs (4800bps);

Valid data bit duration: t2 = 208 × 8 = 1664μs (4800bps);

Stop bit high-level duration: t3 = 208μs (4800bps).

8.1.2.3 Read Timing

The host UART read data sequence is as follows: The host first sends the command byte (0x5, {A4,A3,A2,A1}), followed by the address byte (ADDR) to be read. The BL0973 then sequentially returns the data bytes and finally the checksum byte.

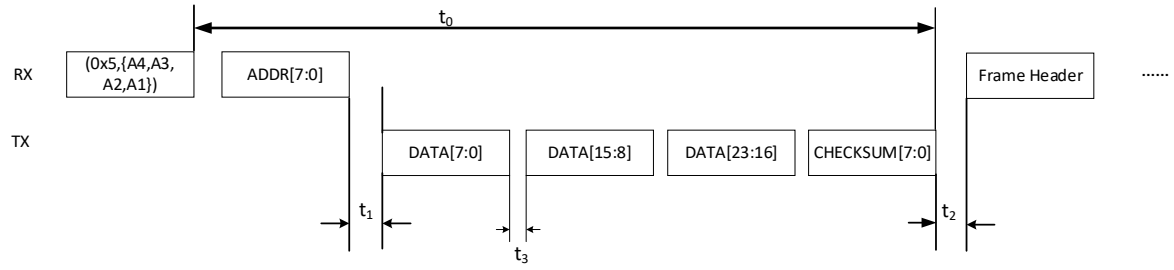


Figure 18 UART Read Timing

(0x5, {A4,A3,A2,A1}) is the frame identification byte for read operations. For example, if A4=A1=1 and A3=A2=0, this pin configuration represents device address 9 (0b1001), making the frame identification byte 0x59.

ADDR corresponds to the internal register address of the BL0973 for the read operation.

The SUM byte is calculated as the bitwise inversion of (Frame ID byte + Addr + Data_L + Data_M + Data_H) & 0xFF.

Table 84 UART Read Timing

	Read Timing Description	**Min**	**Type**	**Max**	**Unit**
t0	Frame length (excluding frame ID byte)			16	mS
t1	Interval between MCU sending register address and BL0910 transmitting data byte		120		uS
t2	Inter-frame gap time	$1t_{bit}$			
t3	BL0910 response byte interval time		$1t_{bit}$		

8.1.2.4 Write Timing

The host UART write data sequence is as follows: The host first sends the command byte (0xA, {A4,A3,A2,A1}), followed by the write address byte (ADDR), then sequentially transmits the data bytes, and finally the checksum byte.

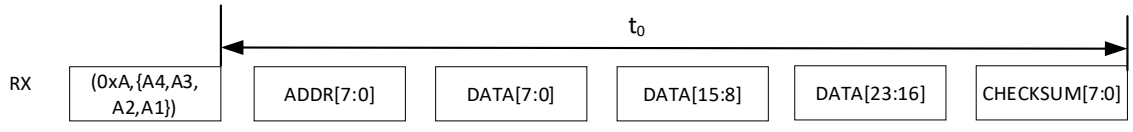


Figure 19 UART Write Timing

(0xA, {A4,A3,A2,A1}) is the frame identification byte for write operations. For example, if A4=A1=1 and A3=A2=0, this pin configuration represents device address 9 (0b1001), making the frame identification byte 0xA9.

ADDR corresponds to the internal register address of the BL0973 for the write operation.

The CHECKSUM byte is calculated as the bitwise inversion of ((Frame ID byte + ADDR + Data_L + Data_M + Data_H) & 0xFF).

Table 85 UART Write Timing Description

	Write Timing Description	Min	Type	Max	Unit
t0	Frame length (excluding frame ID byte)			16	mS

8.1.2.5 UART Interface Protection Mechanism

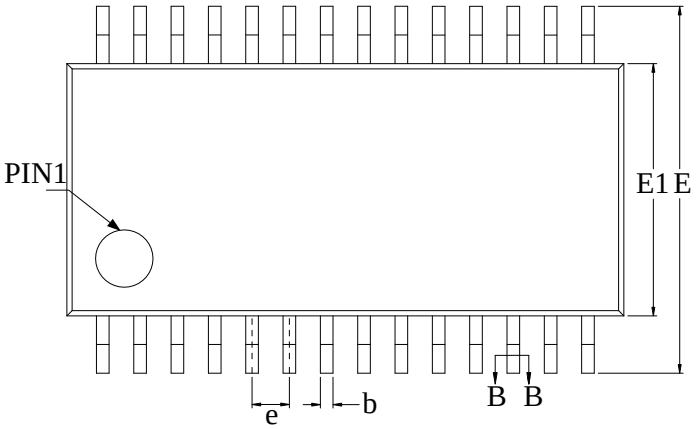
The BL0973's UART communication features a timeout protection mechanism. Upon frame timeout, the UART interface resets. If a read operation fails, wait for >20ms before initiating the next read/write operation.

If frame identification byte errors or CHECKSUM byte errors occur, the current frame data is discarded.

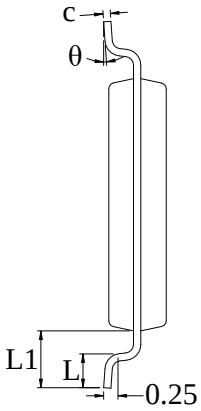
UART module reset: When the RX pin remains at low level for more than 32 t_{bit} (6.67ms at 4800bps) and then pulls high, the UART module resets.

9. Package Information

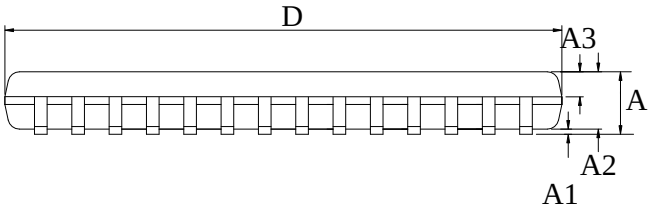
9.1 Outline Dimensions



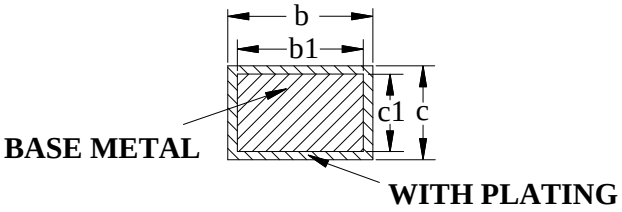
TOP VIEW



SIDE VIEW



SIDE VIEW



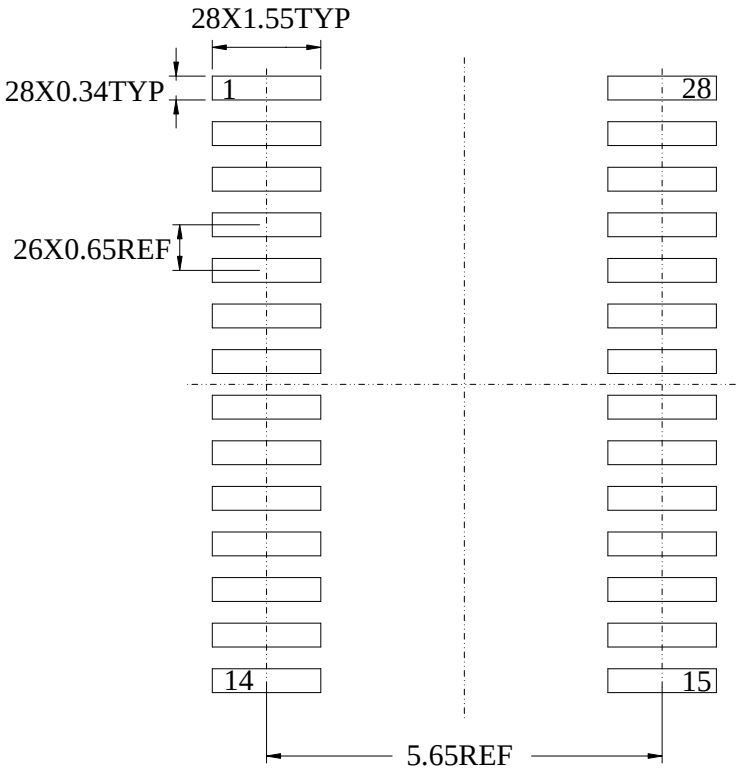
SECTION B-B

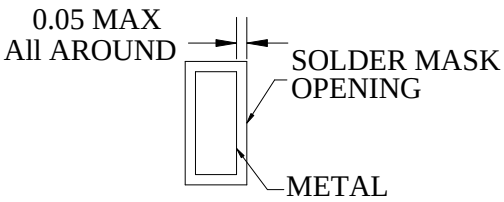
COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	-	0.29
b1	0.19	0.22	0.25
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	8°

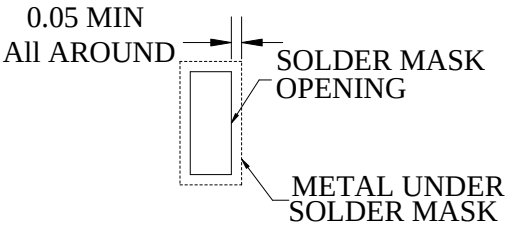
Unit：mm

9.2 Recommended Land Pattern





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit：mm

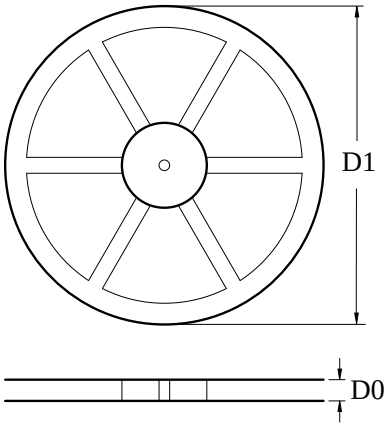
9.3 Marking

Marking Drawing

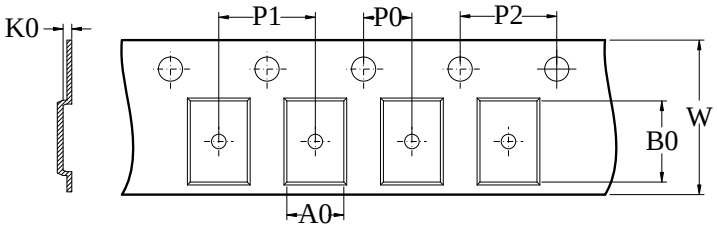
Content	Note
BL0973	Device
YY	The last two digits of the production year
WW	Week of production year
ZZ	Assembly factory code
D86	Laser code
SSSSS	4-8 characters of Lot ID
#	Space, not actually printed

10. Packing Specifications

REEL DIMENSIONS

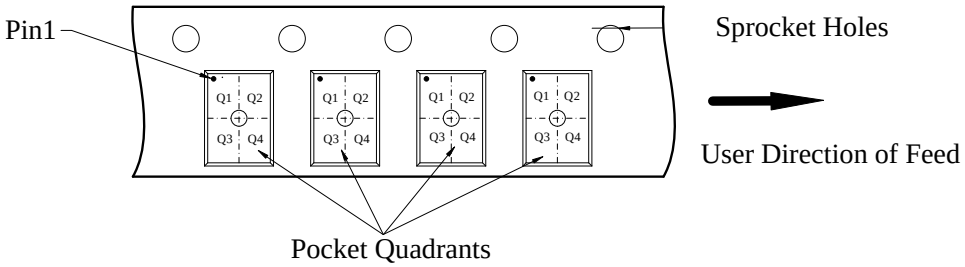


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W： Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

*All dimensions are nominal

Device	Package Type	Pins	SPQ	D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
BL0973	TSSOP	28	3000	330	16	6.7	10	1.3	2	12	4	16	Q1

Revision History

Version	Date	Changes
V01	2024/05/31	Initial version
V02	2024/07/19	Correction and modification
V03	2025/05/22	Modify the description of the output mode register MFX_SEL; Adjust the range and gain settings of the analog input signal; Modify format

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