上海贝岭 SHANGHAI BELLING

BL9362

60V, 2MHz, 600mA Step-Down Converter

GENERAL DESCRIPTION

The BL9362 is a wide input range, high-efficiency, and high frequency DC-to-DC step-down switching regulator, capable of delivering up to 0.6A of output current.

With a fixed switching frequency of 2MHz, this current mode PWM controlled converter allows the use of small external components, such as ceramic input and output caps, as well as small inductors.

Including cold crank and double battery jump-starts, the minimum input voltage may be as low as 4.5V and the maximum up to 60V, with even higher transient voltages. With these high input voltages, linear regulators cannot be used for high supply currents without overheating the regulator. Instead, high efficiency switching regulators such as BL9362 must be used to minimize thermal dissipation.

BL9362 is available SOT23-6 Packages.

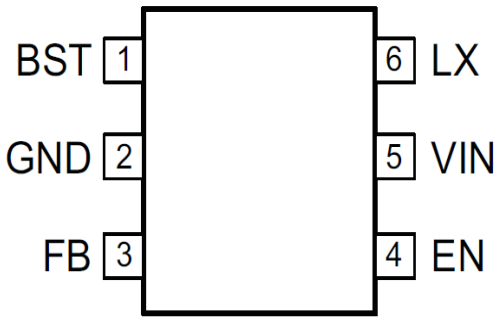
FEATURES

- Wide Input Operating Range from 4.5V to 60V
- 850m Ω internal NMOS
- Up to 95% Efficiency at 16V in 12V out L=47uH with 300mA loading
- Internal compensation
- Capable of Delivering 600mA continuous output current
- Fixed 2MHz PWM operation
- Internal soft start
- Output voltage adjustable down to 0.795V
- Cycle-by-cycle current limit
- Current Mode control
- Short-circuit protection
- Logic Control Shutdown EN can be short to VIN
- Thermal shutdown and UVLO
- Available in SOT23-6 Package

APPLICATIONS

- Smart/Industrial/Power Meters
- Industrial Applications
- Automotive Applications

PIN OUT



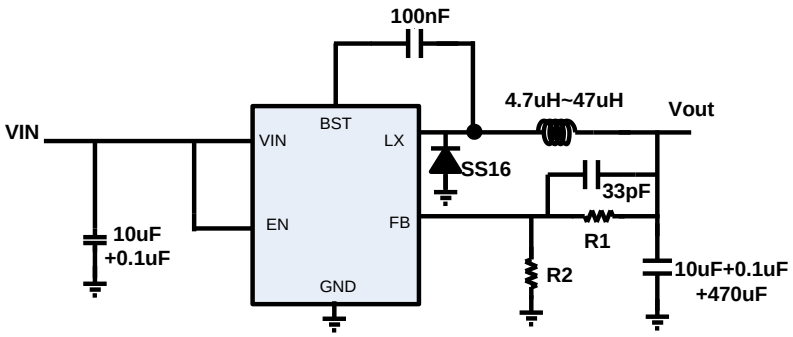
SOT23-6L

(Top View)

PINOUT DESCRIPTION

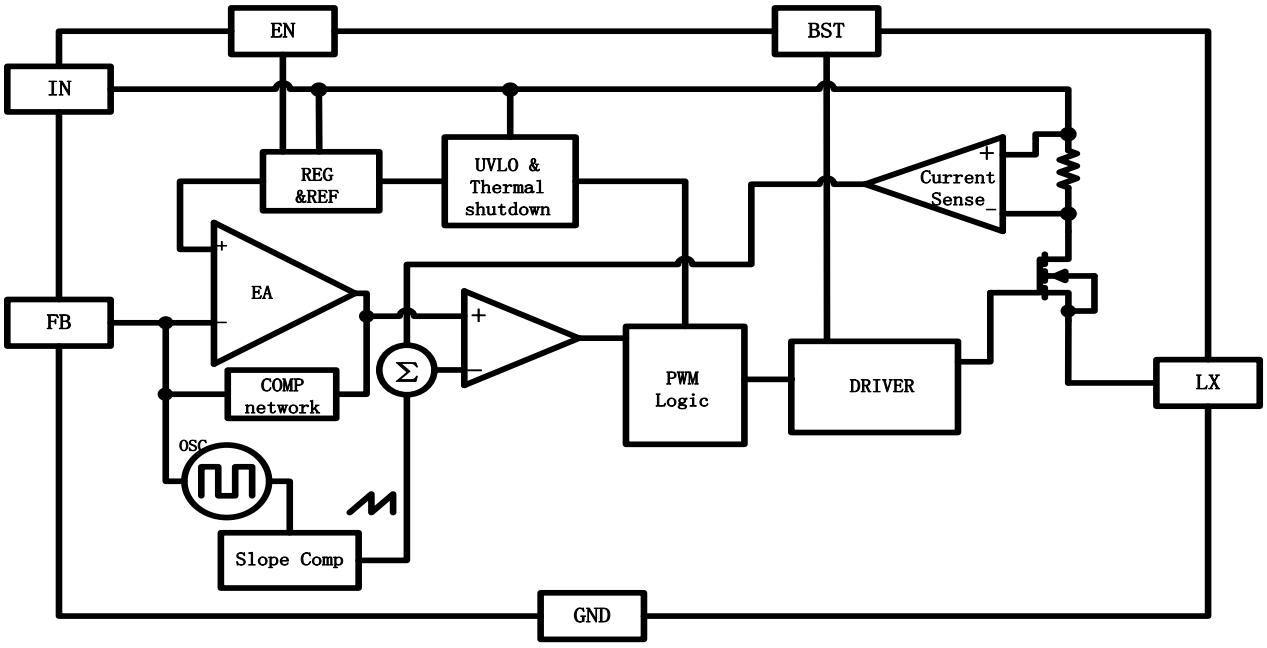
Pin #	Name	Description
1	BST	Bootstrap pin for top Switch. In Typ. application, a 0.1uF or larger capacitor should be connected between this pin and the LX pin to supply current to the top Switch gate and top Switch driver.
2	GND	Analog Ground
3	FB	Output feedback pin. In Typ. application, FB senses the output voltage and is regulated by the control loop to 795mV. Connect a resistive divider at FB.
4	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
5	VIN	Input voltage pin, In Typ. application, VIN supplies power to the IC. Connect a 4.5V to 60V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
6	LX	LX is the Switching node that supplies power to the output Connect the output LC filter from LX to the output load.

TYPICAL APPLICATION



Notice: BL9362 minimum duty cycle = 20%, and the relationship between duty cycle to output voltage and input voltage is duty cycle = output voltage / input voltage, so the maximum input voltage = output voltage / 0.2 to ensure that SW does not cause frequency hopping due to too small duty cycle.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Parameter		Value
Input Voltage Range		-0.3V-65V
Max Operating Junction Temperature(Tj)		150°C
LX, EN Voltage		–0.3V to VIN+0.3V
BST Voltage		–0.3V to LX+6V
FB Voltage		–0.3V to 6V
LX to ground curren		Internally limited
Operating Temperature(To)		-40°C –85°C
Package Thermal Resistance (θjc)	SOT23-6	110°C / W
Storage Temperature(Ts)		-55°C - 150°C
ESD Rating		2500V

Note: Exceed these limits to damage to the device. Exposure to absolute maximum rating conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VIN = VEN = 16V, unless otherwise specified. Typical values are at TA = 25°C .)

SYMBOL	PARAMETER	Test conditions	MIN	TYP	MAX	UNITS
VIN	Input Voltage Range		4.5		60	V
IQ	Input Supply Current	Vfb=5V no loading		648		uA
Isd	Input Shutdown Current	Ven<0.3V		0.2	3	uA
VFB		4.5V<Vin<60V	0.780	0.795	0.810	V
ENABLE						
Ven_ON	En high level	VFB=0V,rising	1.23	2.5		V
Ven_OFF	En low level	VFB=0V,falling		1	1.13	V
En hys	En Hysteresis	VFB=0V		0.10		V
IEN	Enable input current	VEN=16V		4.4		uA
MODULATOR						
Fosc	OSC frequency		1.6	2	2.4	MHz
Dmax				87		%
Ton min	Min on time			100		ns
Ilim	Limited current			0.95		A
Temp	Termal shutdown	Temp rising		160		℃
		Temp falling		140		℃
Power stage output						
Ileakage	NMOS leakage	VEN=0V, VLX=0V			10	uA
RDSON	NMOS on resistance	VIN=12V Vbst-Vlx=5V		850		mΩ

FUNCTIONAL DESCRIPTIONS

Loop Operation

The BL9362 is a wide input range, high-efficiency, DC-to-DC step-down switching regulator, capable of delivering up to 0.6A of output current, integrated with a 850mΩ high side MOSFET. It uses a PWM current-mode control scheme. An error amplifier integrates error between the FB signal and the internal reference voltage. The output of the integrator is then compared to the sum of a current-sense signal and the slope compensation ramp. This operation generates a PWM signal that modulates the duty cycle of the power MOSFETs to achieve regulation for output voltage.

APPLICATION INFORMATION

Setting Output Voltages

Output voltages are set by external resistors. The FB threshold is 0.795V.

RTOP = RBOTTOM × [(VOUT / 0.795) - 1]

Inductor Selection

The peak-to-peak ripple is limited to 30% of the maximum output current. This places the peak current far enough from the minimum over current trip level to ensure reliable operation while providing enough current ripples for the current mode converter to operate stably. In this case, for 0.6A maximum output current, the maximum inductor ripple current is 300 mA. The inductor size is estimated as following equation:

LIDEAL=(VIN(MAX)-VOUT)/IRIPPLE*DMIN*(1/FOSC)

Therefore, for VOUT=5V, The inductor values is calculated to be L = 13µH. Chose 10µH or 15µH

For VOUT =3.3V,The inductor values is calculated to be L = 9.2µH. Chose 10µH

Output Capacitor Selection

For most applications a nominal 22µF or larger capacitor is suitable. The BL9362 internal compensation is designed for a fixed corner frequency that is equal to FC= 8.7KHz

For example, for VOUT=5V, L=15µH, COUT=22µF.

The output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance. Output ripple with a ceramic output capacitor is approximately as follows:

VRIPPLE = IL(PEAK)[1 / (2π x fOSC x COUT)]

If the capacitor has significant ESR, the output ripple component due to capacitor ESR is as follows:

VRIPPLE(ESR) = IL(PEAK) x ESR

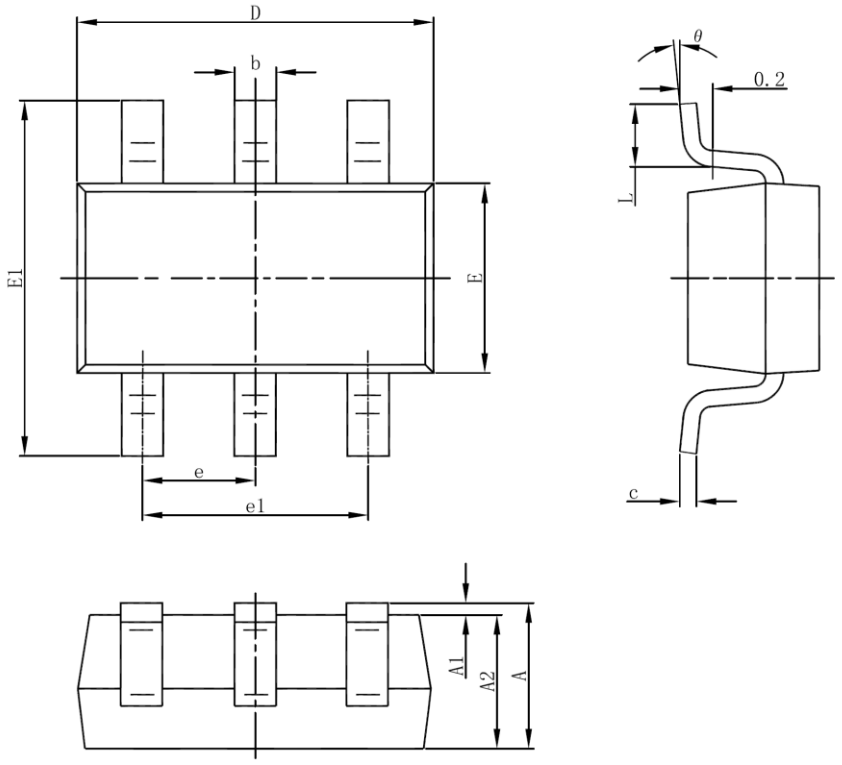
Input Capacitor Selection

The input capacitor in a DC-to-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source. The output capacitor keeps output ripple small and ensures control-loop stability.

Components Selection

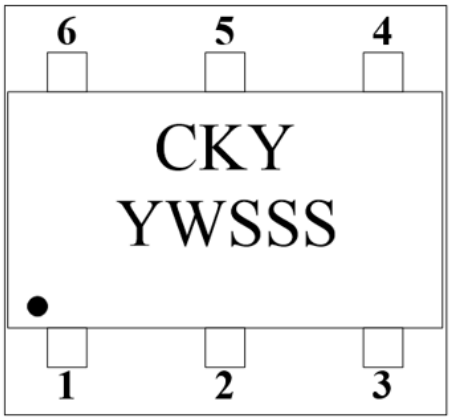
R1(K)	Vo(V)	R2(K)	Recommend
127	12	9.00	9.09K
127	5	23.97	23.7K
127	3.3	40.24	40.2K

PACKAGE OUTLINE

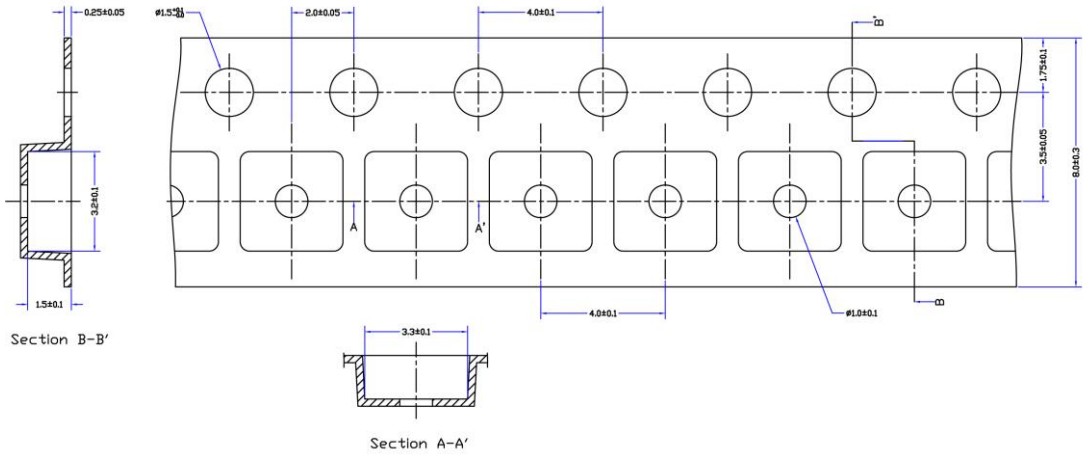


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Marking Diagram



Tray information



Storage conditions and packaging

Humidity sensitivity level：MSL 3
Warranty period：Two years
Packing method：Tape
Minimum packaging：SOT23-6L 3000