Features

- Fully operational to +600 V
- 3 V logic compatible
- Floating channel designed for bootstrap operation
- Gate drive supply range from 10 V to 20 V
- UVLO for both channels
- 2.5A Output Current Capability
- Matched propagation delay for both channels

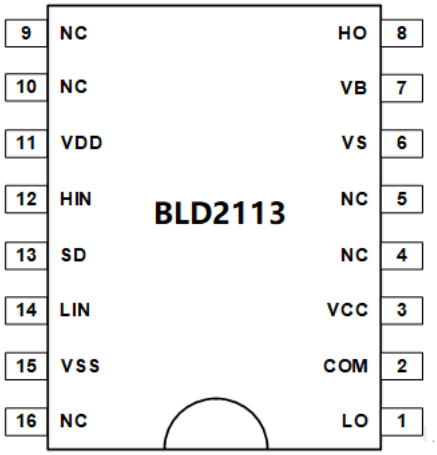
Applications

- High and medium-power motor driver
- Power MOSFET or IGBT driver
- Lighting ballast

Package Options

- SOIC16 (wide body)

Pin Configuration



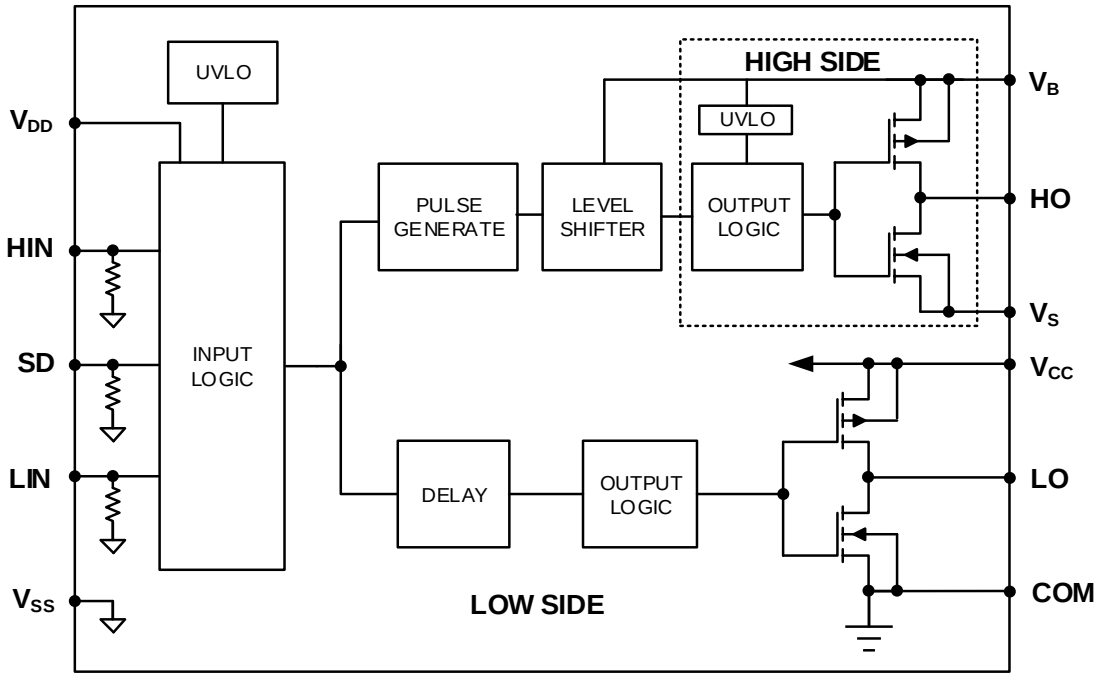
Pin Definitions

PIN NO.	PIN NAME	PIN FUNCTION
1	LO	Low side gate drive output, in phase with LIN
2	COM	Low side return
3	V_{CC}	Low side supply
6	V_S	High side floating supply return
7	V_B	High side floating supply
8	HO	High side gate drive output, in phase with HIN
11	V_{DD}	Logic supply
12	HIN	Logic input for high side gate driver output (HO) , in phase
13	SD	Logic input for shutdown
14	LIN	Logic input for low side gate driver output (LO), in phase
15	V_{SS}	Logic ground

General Description

The BLD2113 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels based on P_SUB P_EPI process. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications.

Functional Block Diagram



Absolute Maximum Ratings

Exceeding these ratings may damage the device.

The absolute maximum ratings are stress ratings only at T_A=25°C, unless otherwise specified.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	-0.3	625	V
V_S	High side floating supply return	V_B - 25	V_B + 0.3	
V_{HO}	High side gate drive output	V_S -0.3	V_B + 0.3	
V_{CC}	Low side supply	-0.3	25	

V_{LO}	Low side gate drive output	-0.3	V_{CC} + 0.3	
V_{DD}	Logic supply	-0.3	V_{CC} + 0.3	
V_{SS}	Logic ground	V_{CC} -25	V_{CC} + 0.3	
V_{IN}	Logic input	V_{SS}-0.3	V_{DD} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	--	50	V/ns
ESD	HBM Model	2.5		kV
	Machine Model	200		V
PD	Package Power Dissipation @ TA ≤25°C (14 Lead DIP)	--	1.6	W
	(16 Lead SOIC)	--	1.25	
R_{thJA}	Thermal Resistance Junction to Ambient (14 Lead DIP)	--	75	°C /W
	(16 Lead SOIC)	--	100	
T_J	Junction Temperature	--	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	--	300	

Recommended Operating Conditions

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	V_S +10	V_S +20	V
V_S	High side floating supply return	COM-8	600	
V_{HO}	High side gate drive output voltage	V_S	V_B	
V_{CC}	Low side supply	10	20	
V_{LO}	Low side gate drive output voltage	0	V_{CC}	
V_{DD}	Logic supply	V_{SS}+3	V_{SS}+20	
V_{SS}	Logic ground	-5	5	
V_{IN}	Logic input voltage(HIN & LIN&SD)	0	V_{DD}	
T_A	Ambient temperature	-40	125	°C

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

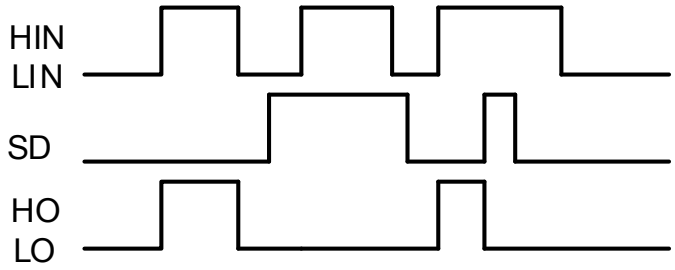
Symbol	Definition	MIN.	TYP.	MAX.	Units
ton	Turn-on propagation delay	-	135	220	ns
toff	Turn-off propagation delay	-	130	220	
tsd	Shutdown propagation delay	-	135	220	
MT	Delay matching	-	-	30	
tr	Turn-on rise time	-	20	30	
tf	Turn-off fall time	-	15	25	

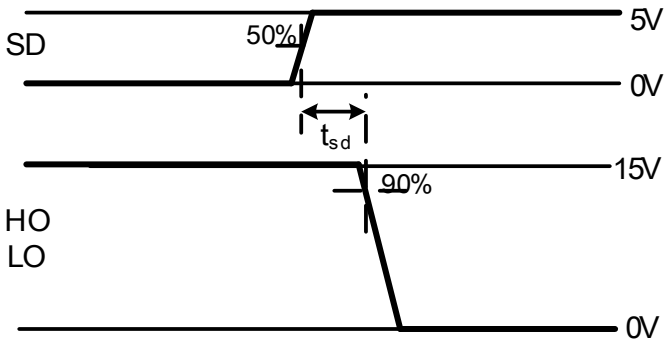
Static Electrical Characteristics

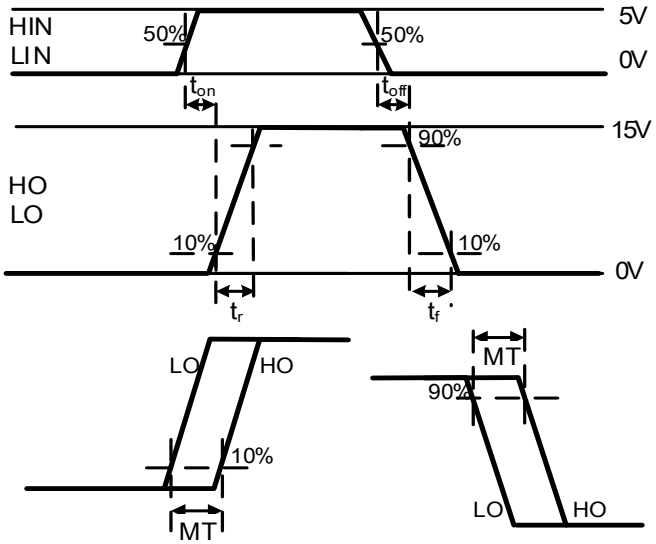
VBIAS (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units
V_{IH}	Logic “1”(HIN & LIN) input voltage	9.5	-	-	V
V_{IL}	Logic “0” (HIN & LIN) input voltage	-	-	5	
V_{OH}	High level output voltage, VBIAS - VO	-	-	1.4	
V_{OL}	Low level output voltage, VO	-	-	0.15	
I_{QDD}	Quiescent VDD supply current	-	-	30	μA
I_{QCC}	Quiescent VCC supply current	-	120	240	
I_{QBS}	Quiescent VB supply current	-	75	150	
I_{LK}	Leakage current from VS(600V) to GND	-	-	10	
I_{IN+}	Logic “1” input bias current	-	20	40	
I_{IN-}	Logic “0” input bias current	-	-	5	
V_{BSU+}	VBS supply UVLO threshold	7.5	8.4	9.7	V
V_{BSU-}		7	8	9.4	
V_{CCU+}	VCC supply UVLO threshold	7.5	8.4	9.6	
V_{CCU-}		7	8	9.4	
I_{O+}	Output high short circuit pulsed current	-	2.5	-	A
I_{O-}	Output low short circuit pulsed current	-	2.5	-	

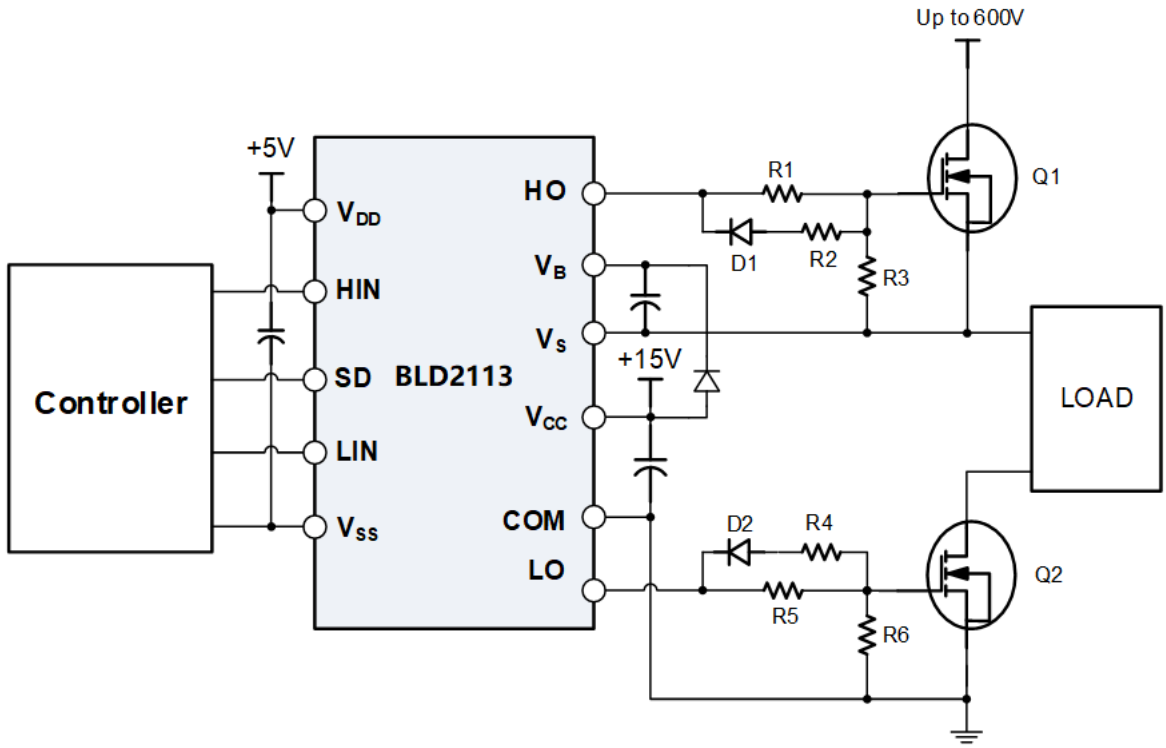
Function Timing Diagram







Typical Application Circuit



Package Information

SOIC16 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	2.65	D	10.10	10.30	10.50
A1	0.10	-	0.30	E	10.26	10.41	10.60
A2	2.25	2.30	2.35	E1	7.30	7.50	7.70
A3	0.97	1.02	1.07	e	1.27BSC		
b	0.35	-	0.44	L	0.55	-	0.85
b1	0.34	0.37	0.39	L1	1.4BSC		
c	0.25	-	0.31	θ	0	-	8°
c1	0.24	0.25	0.26				

SOIC16 Package Outlines