上海贝岭
SHANGHAI BELLING

BLL2206

6A 4MHz 5.5V Synchronous Buck Converter

DESCRIPTION

The BLL2206 is a high-efficiency, DC-to-DC step-down switching regulators, capable of delivering up to 6A of output current. The device operates from an input voltage range of 2.3V to 5.5V and provides an output voltage from 0.55V to 3.3V.

The BLL2206 works at a nominal fixed frequency of 4MHz which allows the use of small external components, such as ceramic input and output capacitors, as well as small inductors, while still providing low output ripples. Efficiency is maximized through the integrated 11.5mΩ/6.5mΩ MOSFETs. Using PFM mode in light load and PWM mode in heavy load makes the BLL2206 keep high efficiency in full range. Low noise output along with excellent efficiency makes BLL2206 an ideal replacement for large power consuming linear regulators.

The BLL2206 includes under-voltage lockout, current limiting, short-circuit protection and thermal shutdown protection.

The BLL2206 is available in small DFN-9 package which size is 3mm*2mm*0.75mm.

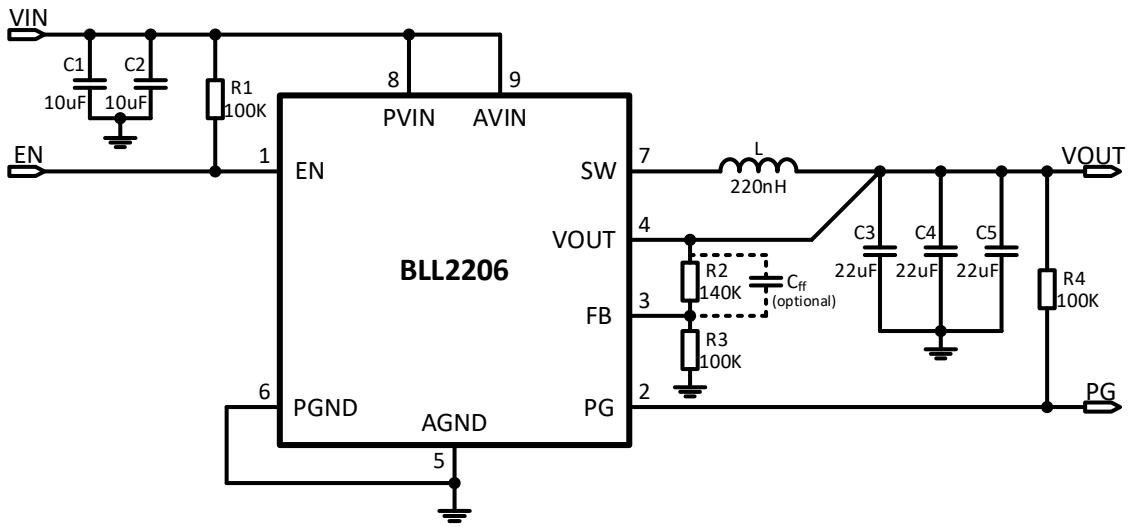
FEATURES

- 2.3V to 5.5V input voltage
- 6A continuous output current
- High efficiency: up to 98%
- 4MHz switching frequency
- PFM mode in light load
- Accurate reference: 0.5V
- Low dropout 100% duty operation
- Integrated soft-start
- Fast load transient response
- Hiccup short-circuit protection
- Output discharge function
- Input under-voltage lockout
- Over current protection
- Over temperature protection
- Pb free & RoHS

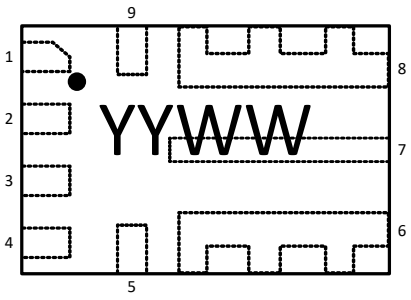
APPLICATIONS

- Low-voltage, high-density power systems
- Communications infrastructure
- IOT

TYPICAL APPLICATION



ORDERING INFORMATION

Mark Explanation		Ordering Information	
YY: Date code (Year) WW: Date code (Week)		Product ID	BLL2206CKMATR
		Package	DFN3x2-9
		Devices per reel	5000pcs

PIN DESCRIPTION

Pin	Name	Description
1	EN	Enable. Part is active when V_{EN} >1.2V. Part is disabled when V_{EN} <0.4V.
2	PG	Power Good. Connect to VOUT through resistor.
3	FB	Feedback. Connect to the mid-point of external resistor divider to set the desired V_{OUT}.
4	VOUT	Output voltage sensing pin.
5	AGND	Analog ground.
6	PGND	Power ground. Low-side switch source terminal.
7	SW	Switching node. Connect to the output inductor.
8	PVIN	Power supply input. Connect to power source with a minimum 10uF ceramic capacitor.
9	AVIN	Power supply for control section. Connect to PVIN.

ABSOLUTE MAXIMUM RATING

Parameter	Min	Max	Units
DC supply voltage, VIN	-0.3	7.0	V
SW	-0.3	V_{IN} +0.3	V
SW (10ns transient)	-4.0	8.0	V
Voltage on other pins, FB, EN, PG, VOUT	-0.3	V_{IN} +0.3	V
Storage temperature range	-40	150	°C
Junction temperature	-40	150	°C
Electrostatic discharge (HBM)	-4000	4000	V
Electrostatic discharge (CDM)	-2000	2000	V

Note: *Operation of the device outside of these parameters may cause permanent damage.*

RECOMMENDED WORK CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage	V_{IN}	2.3		5.5	V
Output current	I_{OUT}	0		6	A
Output inductor	L		220		nH
Input capacitor	C_{IN}		2*10		µF
Output capacitor	C_{OUT}		3*22		µF
Operating temperature, junction	T_J	-40		125	°C

THERMAL RESISTANCE INFORMATION

Junction to ambient thermal resistance is a function of board layout and ambient air flow condition. This data is based on four layers PCB (30mm x 30mm; 70µm Cu top signal layer) in still air box in accordance with JEDEC standard JESD51 on natural convection.

Parameter	Symbol	Typ	Units
Junction-to-ambient thermal resistance	θ_{JA}	30.5	°C/W
Junction-to-case thermal resistance	θ_{JC}	16.7	°C/W

ELECTRICAL CHARACTERISTICS

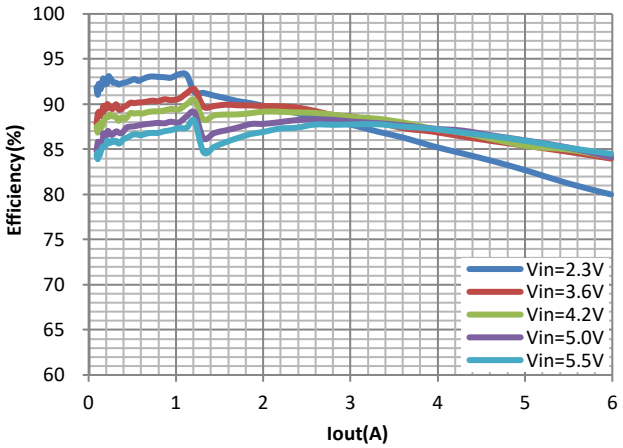
Typical values unless otherwise noted: V_{IN} =3.6V, V_{OUT} =1.8V, T_A =25°C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
DC Characteristics						
Supply voltage	V_{IN}		2.3		5.5	V
Quiescent current	I_Q	PFM mode		1		mA
		No load, no switching		50		μA
Shutdown current	I_{SHDN}	EN=GND		0.1	3.5	μA
Under-voltage lockout threshold	V_{UVLO}	Rising V_{IN}		2.1	2.2	V
Under-voltage lockout hysteresis	$V_{UVLOHYST}$			220	250	mV
Thermal shutdown	T_{SD}			155		°C
Thermal shutdown hysteresis	T_{HYST}			30		°C
Logic input: EN						
Logic high voltage	V_{ENH}		1.2			V
Logic low voltage	V_{ENL}				0.4	V
Logic pin leakage current	I_{EN}			2.5		μA
Logic pin hysteresis	V_{ENHYST}			220		mV
Output Characteristics						
Switching frequency	F_{SW}		3.6	4	4.4	MHz
Feedback Voltage (PFM mode)	V_{FB}		0.490	0.5	0.510	V
Feedback Voltage (PWM mode)			0.495	0.5	0.505	
Input leakage current into FB pin	$I_{FB, LKG}$				0.1	μA
Soft-start time	T_{SS}			3		ms
Enable turn-on delay	T_{EN}			100		μs
Power Switches						
PMOS on resistance	R_{DSONP}	V_{IN} =V_{GS} =3.6V	9.5	11.5	15	mΩ
NMOS on resistance	R_{DSONN}	V_{IN} =V_{GS} =3.6V	5	6.5	8	mΩ
PMOS peak current limit	I_{LIM}	V_{IN} =3.6V, open loop		8		A
Output discharge resistance	R_{DIS}	EN=GND		16		Ω
Power Good						
PG threshold V_{OUT} rising	V_{PGR}			98		%
PG threshold V_{OUT} falling	V_{PGF}			94		%
PG low voltage	V_{PGL}	Sink current=1mA			100	mV
Input leakage current into PG pin	$I_{PG, LKG}$				0.1	μA

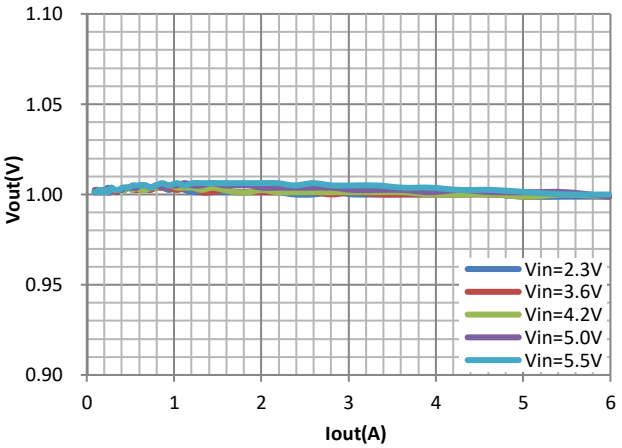
ELECTRICAL PERFORMANCE

Typical test conditions unless otherwise noted: C_{IN}=2*10uF, L=220nH, C_{OUT}=3*22uF, F_{SW}=4MHz and T_A=25°C.

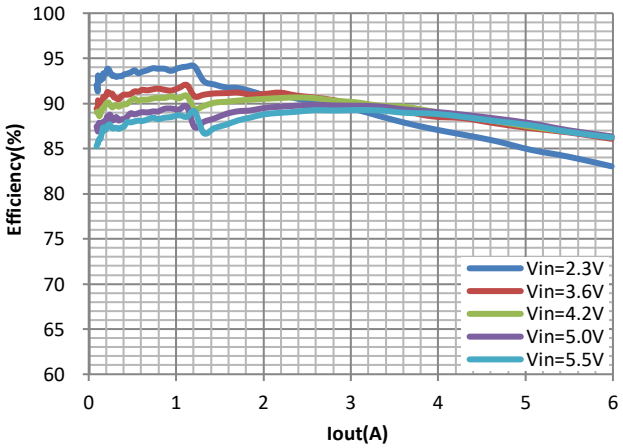
Efficiency vs. Output Current
(Vout=1.0V)



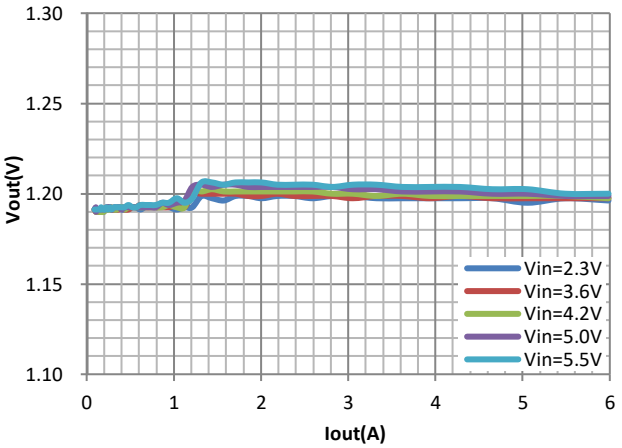
Load Regulation
(Vout=1.0V)



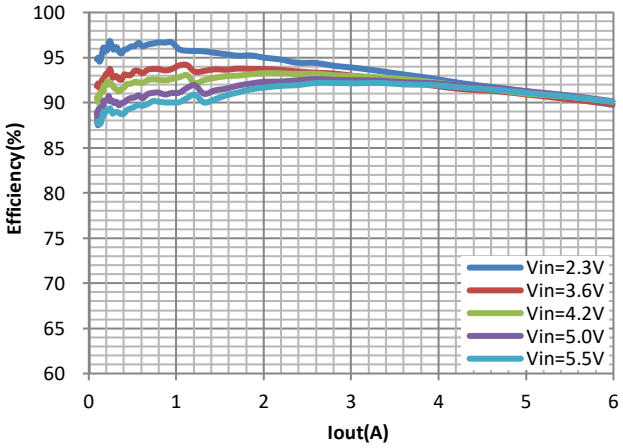
Efficiency vs. Output Current
(Vout=1.2V)



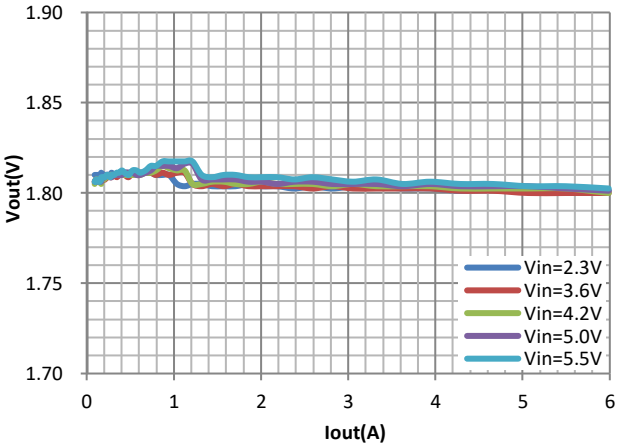
Load Regulation
(Vout=1.2V)



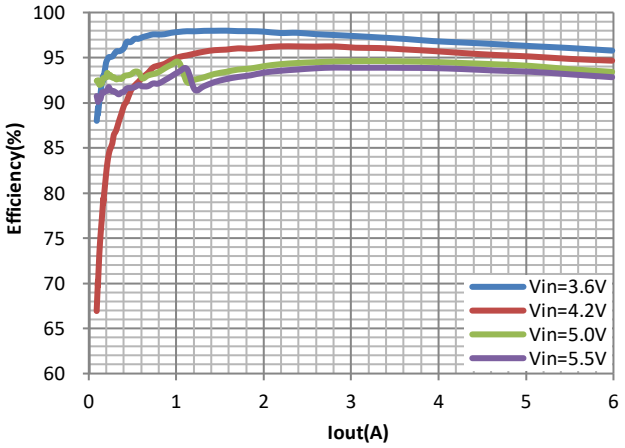
Efficiency vs. Output Current
(Vout=1.8V)



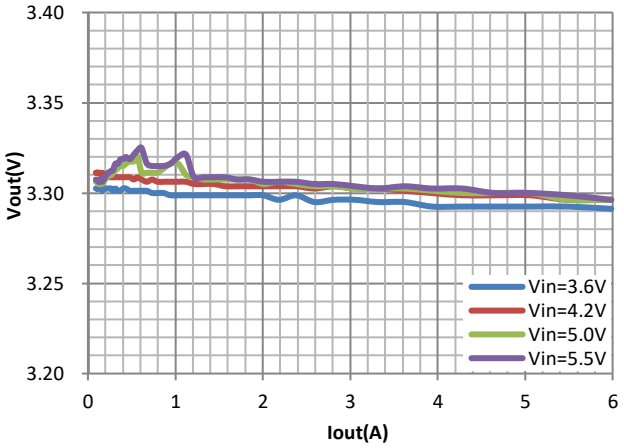
Load Regulation
(Vout=1.8V)



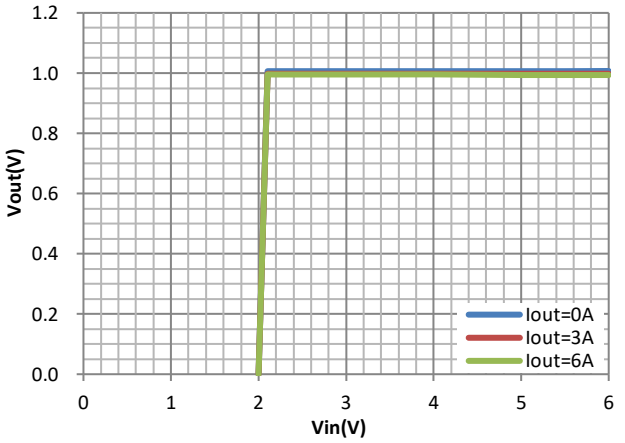
Efficiency vs. Output Current
(Vout=3.3V)



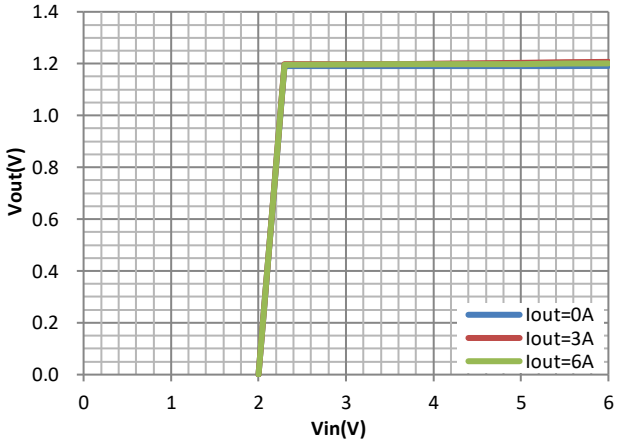
Load Regulation
(Vout=3.3V)



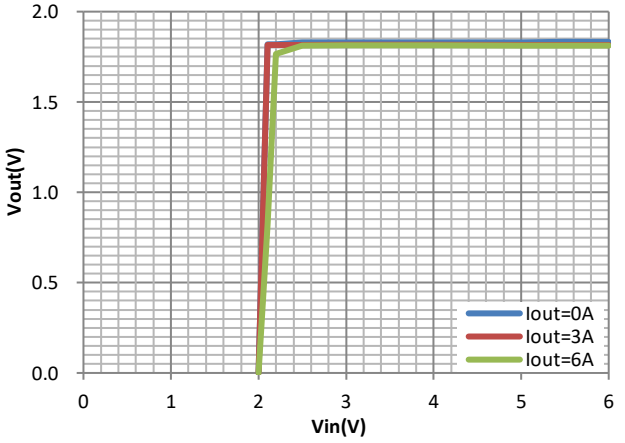
Line Regulation
(Vout=1.0V)



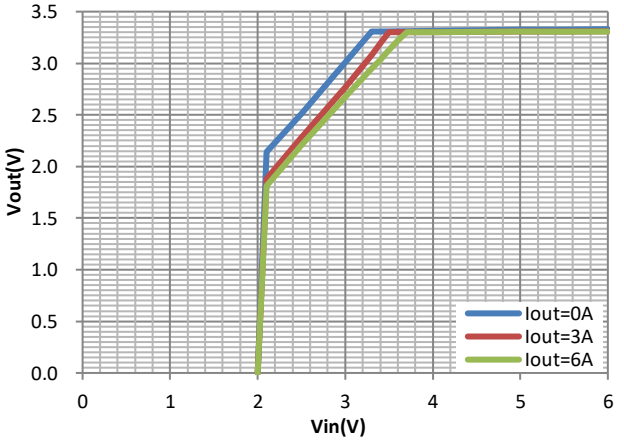
Line Regulation
(Vout=1.2V)



Line Regulation
(Vout=1.8V)

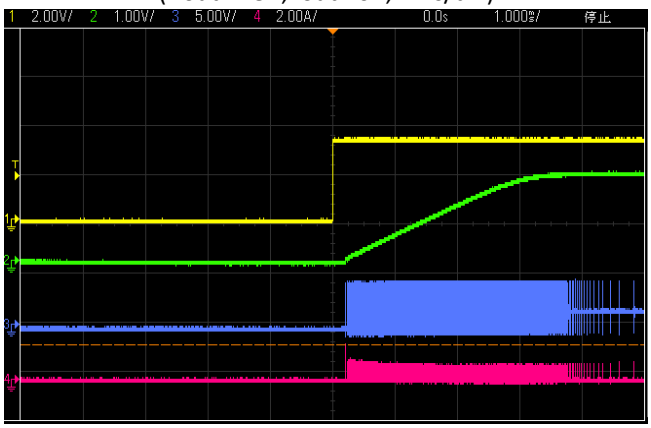


Line Regulation
(Vout=3.3V)



EN Power On

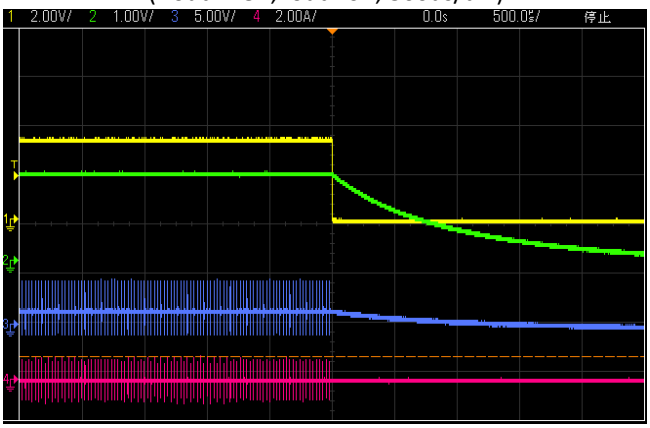
(Vout=1.8V, Iout =0A, 1ms/div)



Ch1—EN(2V/div), Ch2—Vout(1V/div),
Ch3—SW(5V/div), Ch4—I_L(2A/div)

EN Power Off

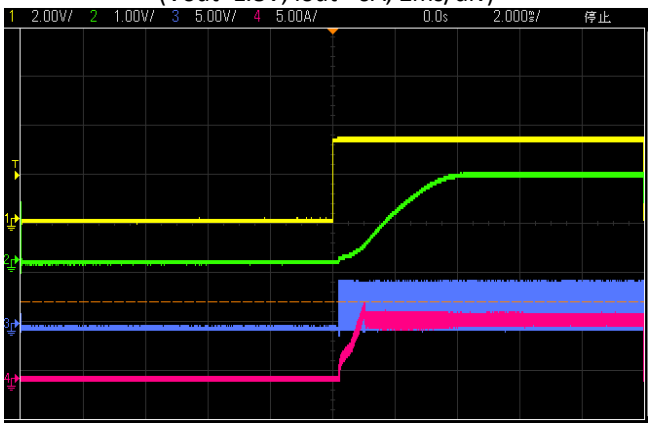
(Vout=1.8V, Iout =0A, 500us/div)



Ch1—EN(2V/div), Ch2—Vout(1V/div),
Ch3—SW(5V/div), Ch4—I_L(2A/div)

EN Power On

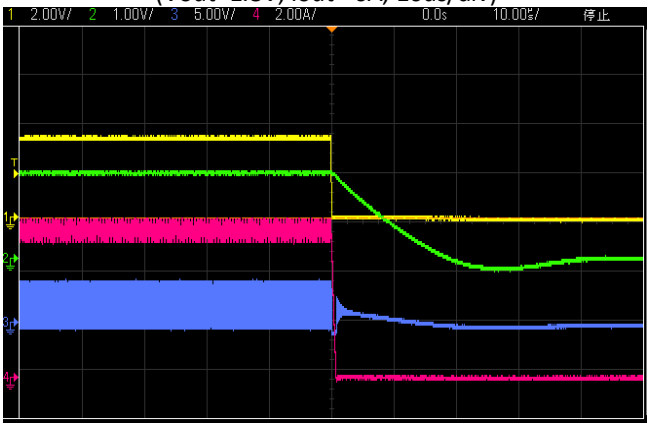
(Vout=1.8V, Iout =6A, 2ms/div)



Ch1—EN(2V/div), Ch2—Vout(1V/div),
Ch3—SW(5V/div), Ch4—I_L(5A/div)

EN Power Off

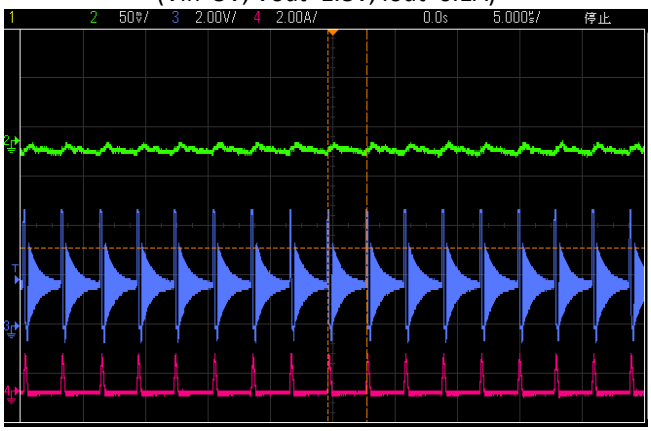
(Vout=1.8V, Iout =6A, 10us/div)



Ch1—EN(2V/div), Ch2—Vout(1V/div),
Ch3—SW(5V/div), Ch4—I_L(2A/div)

Output Ripple Wave

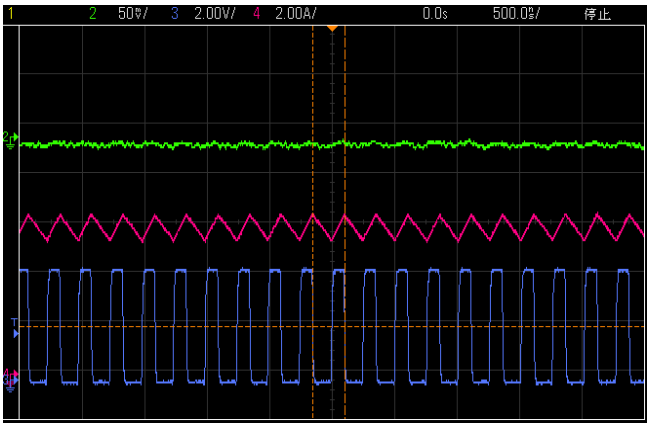
(Vin=5V, Vout=1.8V, Iout=0.1A)



Ch2—Vout_ripple(50mV/div),
Ch3—SW(2V/div), Ch4—I_L(5A/div)

Output Ripple Wave

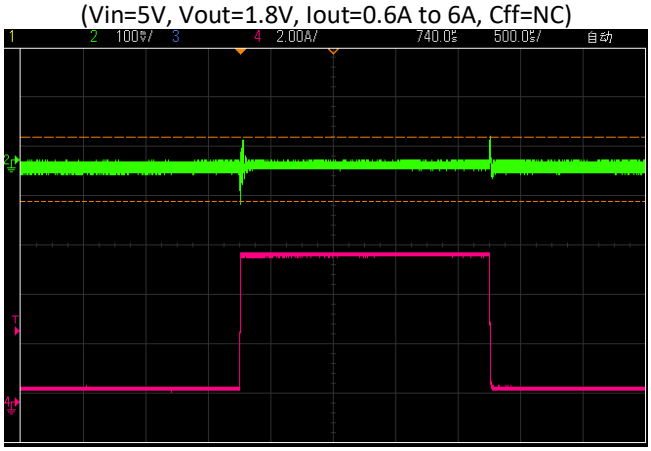
(Vin=5V, Vout=1.8V, Iout=6A)



Ch2—Vout_ripple(50mV/div),
Ch3—SW(2V/div), Ch4—I_L(5A/div)

Load Transient

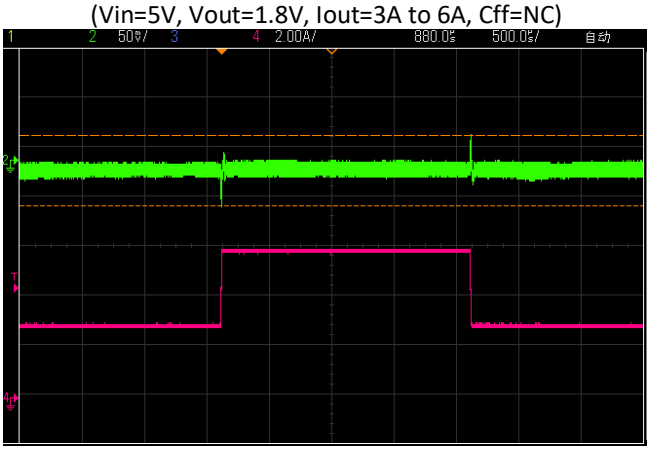
(Vin=5V, Vout=1.8V, Iout=0.6A to 6A, Cff=NC)



Ch2—Vout_ripple(100mV/div), Ch4—Iout(2A/div)

Load Transient

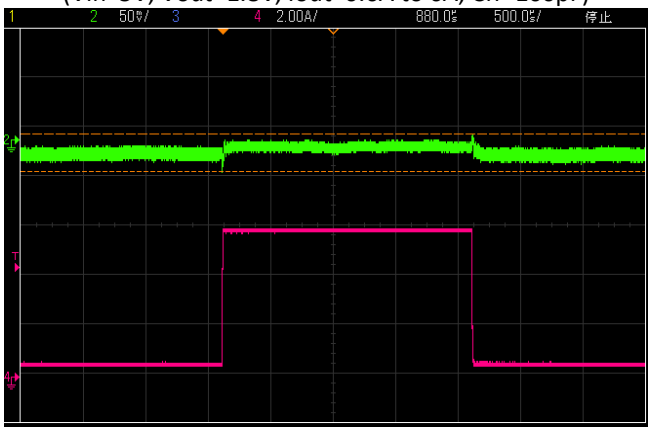
(Vin=5V, Vout=1.8V, Iout=3A to 6A, Cff=NC)



Ch2—Vout_ripple(50mV/div), Ch4—Iout(2A/div)

Load Transient

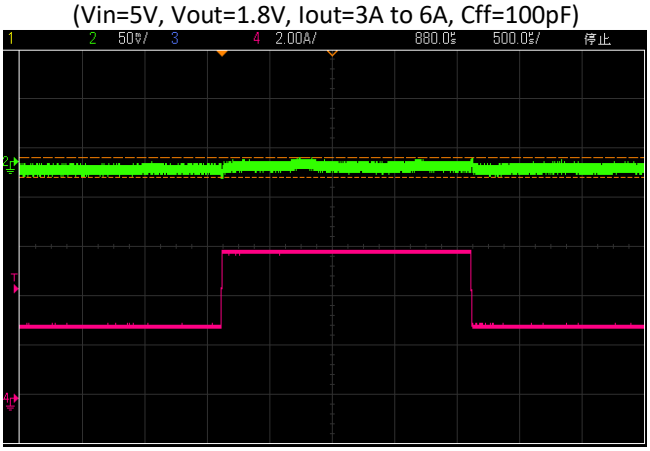
(Vin=5V, Vout=1.8V, Iout=0.6A to 6A, Cff=100pF)



Ch2—Vout_ripple(50mV/div), Ch4—Iout(2A/div)

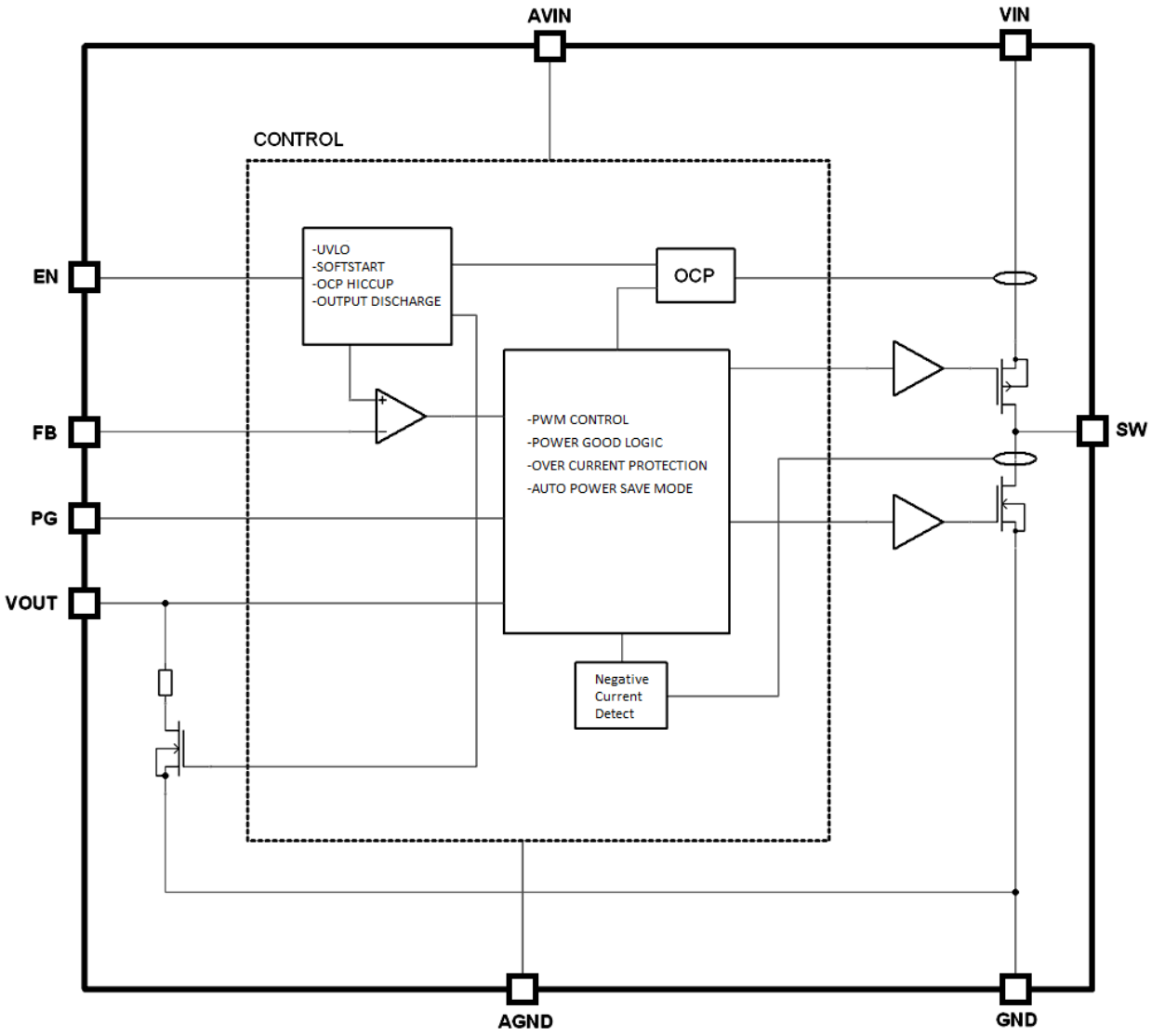
Load Transient

(Vin=5V, Vout=1.8V, Iout=3A to 6A, Cff=100pF)



Ch2—Vout_ripple(50mV/div), Ch4—Iout(2A/div)

BLOCK DIAGRAM



DETAILED DESCRIPTION

The BLL2206 is a synchronous DC/DC voltage regulator available with typical switching frequency of 4MHz. Operating from an input voltage between 2.3V and 5.5V, the regulator can deliver up to 6A of load current.

Enable

Setting the EN pin to logic High enables the device. Alternatively, the device is disabled when the EN voltage is set to logic Low. In this state the IC draws less than 1μA of current and the output is pulled to ground through a resistive load. V_{OUT} starts to ramp up after 100μs delay.

Soft-start

When the device is enabled, internal soft-start circuitry causes V_{OUT} to ramp up over a period of 3ms to limit inrush current. This feature protects a high impedance source from being pulled to a lower voltage as the device turns on.

Under-voltage lockout (UVLO)

The under-voltage lockout feature prevents the device from turning on if V_{IN} is below the UVLO level of 2.1V. If the device is enabled under UVLO conditions, the circuitry will not turn on until the input voltage is increased. Once active, the UVLO circuit has 220mV of hysteresis and the device will turn off if V_{IN} drops below 1.9V.

Active output discharge

When the device is disabled through the EN pin, a discharge path for the output capacitor is created between V_{OUT} and ground through a 16Ω resistor (R_{DIS}).

Modes of operation

The converter automatically switches to pulse frequency modulation (PFM) operation at light current loads. In PFM mode the frequency of pulses is varied to deliver the best possible efficiency. The device switches between PFM and PWM as the load current changes and thus optimizes performance.

If the input voltage ever gets too close to the target output voltage, such that regulation can no longer be maintained, the regulator will enter 100% duty cycle mode. In this mode the high-side switch is ON, connecting the input and output together to deliver a voltage as close to the target as possible.

Thermal shutdown

The device thermal shutdown protection is enabled if the chip temperature exceeds 155°C. Once the temperature drops below 125°C, the device will be re-enabled, and a new soft-start cycle will begin.

Overcurrent protection

The device has overcurrent protection to prevent damage to the device and inductor during overcurrent conditions.

Peak current protection occurs at 8A. After hitting 16 consecutive cycles of peak current limit, the output will be disabled. After being disabled for 1.5ms, the device will be re-enabled, and a new soft-start cycle will begin.

Power Good indicator

The PG pin is an open-drain output and pulls the PG pin low when the FB voltage is less than 94% of the nominal internal reference voltage and resumes when FB voltages is greater than 98% of the nominal internal reference voltage.

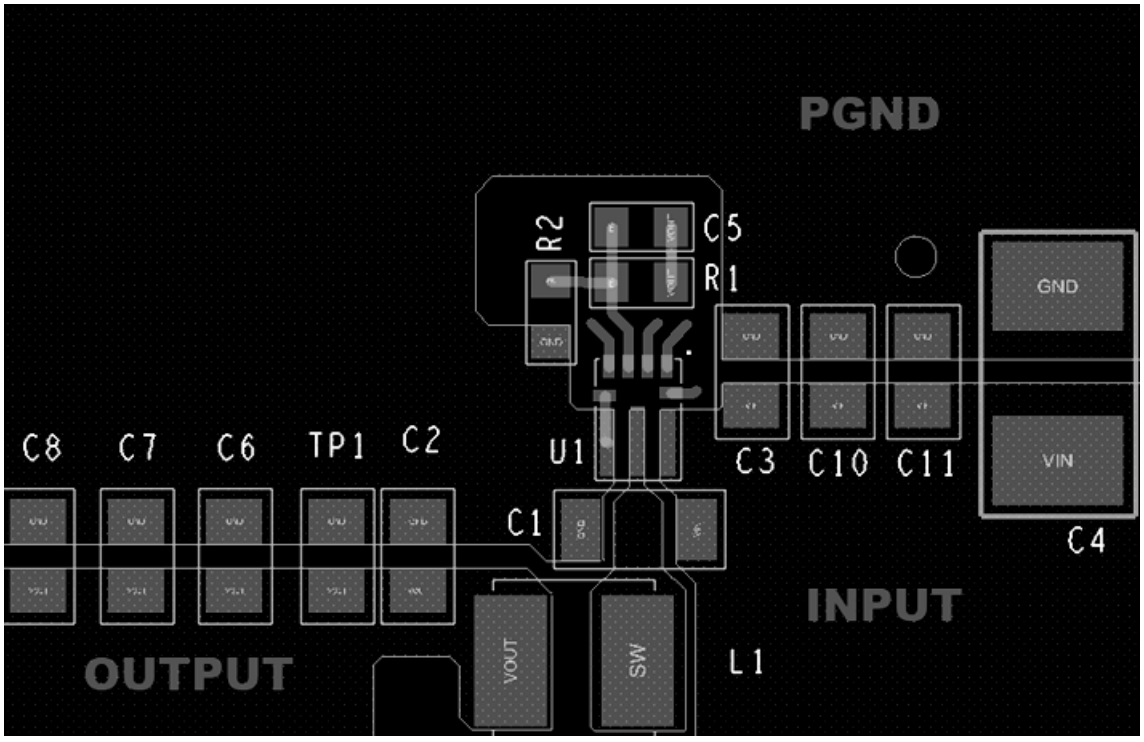
PCB LAYOUT

A well-designed and manufactured PCB is important for all switching power supplies, especially for those operate at high switching frequency.

If the layout is not fulfilled carefully, not only regulator performance could be degraded but also stability or EMI issue may be introduced. Hence, care must be taken in board layout to achieve the specified performance.

Please use the following guidelines when designing PCBs:

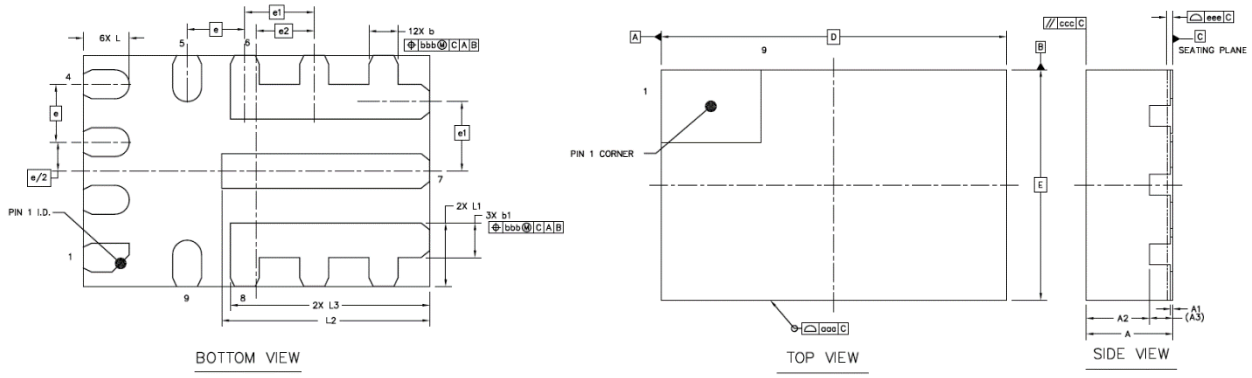
1) Keep components placement as compact as possible.
2) Place a low-ESR input capacitor as close to VIN and GND as possible.
3) Minimize the area between SW pin trace and inductor to limit high frequency radiation.
4) Keep FB trace away from noisy components and traces (e.g., SW and inductor).
5) Use wide and short traces for the main current paths.
6) Ground pins of regulator must be strongly connected to PCB ground with low inductance and impedance.
7) Place common and unbroken ground for CIN and COUT.
8) Reduce excessive thermal relief vias and keep them away from SW and inductor.



PACKAGE OUTLINE

Package	DFN3x2-9	Devices per reel	5000pcs

Package dimension:



Symbol	Dimensions in mm		
	Min	Nom	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2	-	0.55	-
A3		0.203 REF	
b	0.2	0.25	0.3
b1	0.25	0.3	0.35
D		3 BSC	
E		2 BSC	
e		0.5 BSC	
e1		0.6 BSC	
e2		0.5 BSC	
L	0.3	0.4	0.5
L1	0.5	0.55	0.6
L2	1.75	1.8	1.85
L3	1.675	1.725	1.775
aaa		0.1	
ccc		0.1	
eee		0.05	
bbb		0.1	