上海贝岭
SHANGHAI BELLING

BLL2310C

1MHz, 18V, 2A Synchronous Step-Down Converter

DESCRIPTION

The BLL2310C is a high-efficiency, fully integrated, DC-to-DC step-down switching regulators, capable of delivering up to 2A of output current. This device offers two operation modes, PWM and PFM switching control modes, which allows a high efficiency over the wider range of the load.

The BLL2310C guarantees robustness with hiccup-mode output short-circuit protection, cycle-by-cycle current limit, input voltage protection, under voltage lockout and thermal shutdown.

The BLL2310C requires a minimum number of readily available standard external components and is available in a 6-pin SOT23 ROHS compliant package.

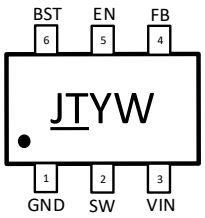
FEATURES

- High efficiency: up to 96%
- 1MHz frequency operation
- 2A output current
- No Schottky diode required
- 4.5V to 18V input voltage range
- 0.8V reference
- Slope compensated current mode control for excellent line and load transient response
- Integrated internal compensation
- Stable with low ESR ceramic output capacitors
- Over current protection with hiccup-mode
- Thermal shutdown
- Inrush current limit and soft start
- Available in SOT23-6
- -40°C to +85°C temperature range

APPLICATIONS

- Distributed power systems
- Digital set top boxes
- Flat panel television and monitors
- Wireless and DSL modems
- Notebook computer

ORDERING INFORMATION

Mark Explanation		Ordering Information	
JT: Product Code YW: Date code (Year & Week)		Product ID	BLL2310CCB6TR
		Package	SOT23-6
		Devices per reel	3000pcs

TYPICAL APPLICATION

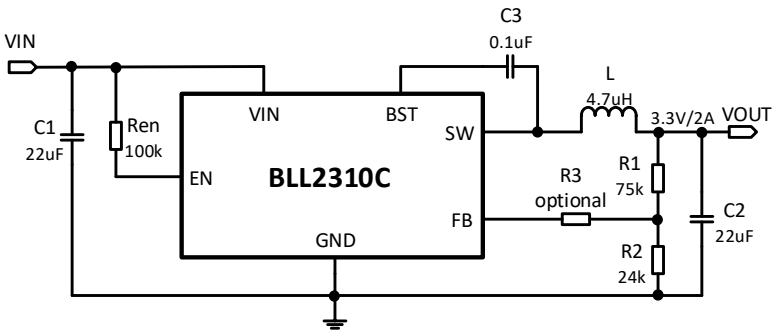


Figure 1.

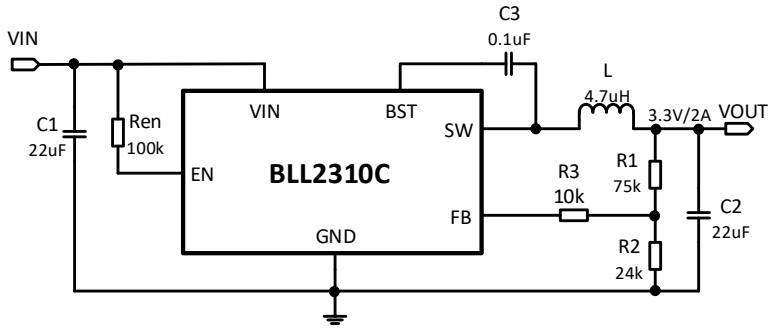


Figure 2.

Table1. Recommended component values

V_{IN}=12V, the recommended BOM list is shows as below.

VOUT	L(uH)	C1(uF)	C2(uF)	C3(uF)	R3(Ω)	R1(Ω)	R2 min(Ω)
1.2	1.0~2.2	10~22	10~22	0.1~1	10K/0	180K	360K
1.5	1.0~2.2	10~22	10~22	0.1~1	10K/0	130K	150K
1.8	1.0~6.8	10~22	10~22	0.1~1	10K/0	150K	120K
2.5	2.2~10	10~22	10~22	0.1~1	10K/0	91K	43K
3.3	2.2~10	10~22	10~22	0.1~1	10K/0	75K	24K
5	2.2~10	10~22	10~22	0.1~1	10K/0	68K	13K

Note:

1) C1 and C2 recommended using 22uF ceramic capacitors. If the electrolytic capacitor is used, it is recommended that the ceramic capacitor in parallel with a capacitance value of 0.1uF or more.

2)The resistance values of R1 and R2 should not be less than recommended values, R3 can be added to enhance stability.

PIN DESCRIPTION

Pin #	Name	Description
1	GND	Ground.
2	SW	Switching pin.
3	VIN	Power supply pin.
4	FB	Adjustable version feedback input. Connect FB to the center point of the external resistor divider.
5	EN	Drive this pin to a logic-high to enable the IC. Drive to a logic-low to disable the IC and enter micro-power shutdown mode.
6	BST	Supply input for the high-side FET gate drive circuit. Connect 0.1µF capacitor between BST and SW pins.

ABSOLUTE MAXIMUM RATING

Parameter		Value
Supply voltage V_{IN}		-0.3V to 19V
Switch node voltage V_{SW}		-0.3V to (V_{IN}+0.3V)
Boost voltage V_{BST}		V_{SW}-0.3V to V_{SW}+5V
Enable voltage V_{EN}		-0.3V to 19V
All other pins		-0.3V to 6V
Package thermal resistance (θ_{JA})	SOT23-6	200°C/W
Package thermal resistance (θ_{JC})		100°C/W
Max operating junction temperature(T_J)		150°C
Storage temperature range		-65°C to 150°C
Lead temperature (Soldering, 10s)		260°C, 10s

RECOMMENDED WORK CONDITIONS

Parameter	Value
Input voltage range	4.5V to 18V
Ambient temperature(T_A)	-40°C to 85°C

ELECTRICAL CHARACTERISTICS

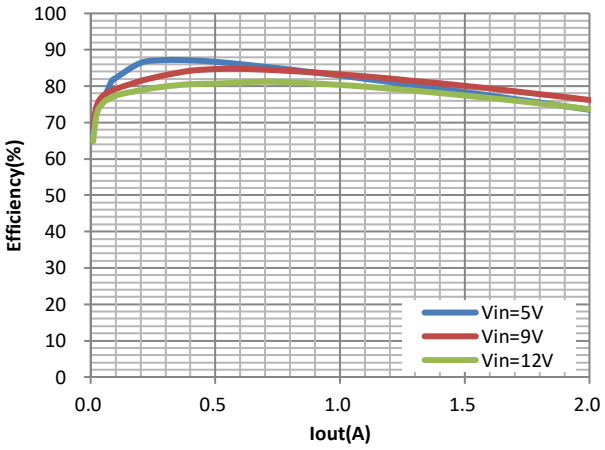
V_{IN}=12V, V_{OUT}=5V, T_A=25°C, unless otherwise stated.

Parameter	Conditions	Min	Typ	Max	Units
Input voltage range		4.5		18	V
UVLO threshold	V_{IN} rising		4.1		V
UVLO hysteresis	V_{IN} falling		100		mV
Supply current in operation	V_{EN} = 2.0V, V_{FB} = 1.1V		0.5		mA
Supply current in shutdown	V_{EN} = 0V or V_{EN} = GND		5	10	uA
Regulated feedback voltage	5V≤V_{IN} ≤16V	0.784	0.8	0.816	V
High-side switch on resistance	V_{BST-SW} = 5V		120		mΩ
Low-side switch on resistance	V_{IN} = 5V		80		mΩ
High-side switch leakage current	V_{EN} = 0V, V_{SW} = 0V		0	10	uA
Upper switch current limit	Minimum duty cycle		3.3		A
Oscillation frequency			1M		Hz
Maximum duty cycle	V_{FB} = 0.7V		92		%
Minimum duty cycle			10		%
Soft start time			1.8		ms
EN input voltage “H”		1.5			V
EN input voltage “L”				0.6	V
Thermal shutdown			150		°C
Thermal shutdown hysteresis			20		°C

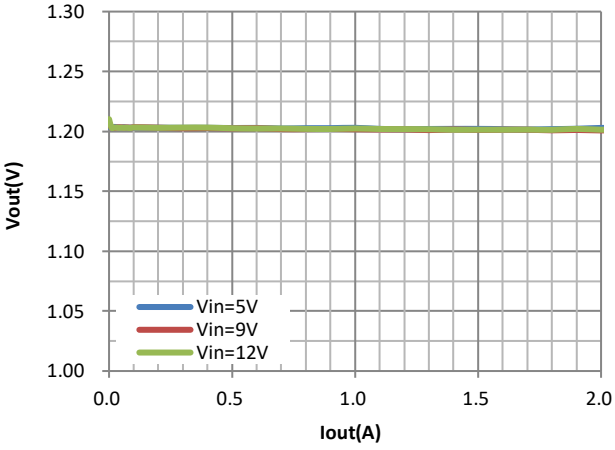
ELECTRICAL PERFORMANCE

Tested under T_A=25°C, unless otherwise specified.

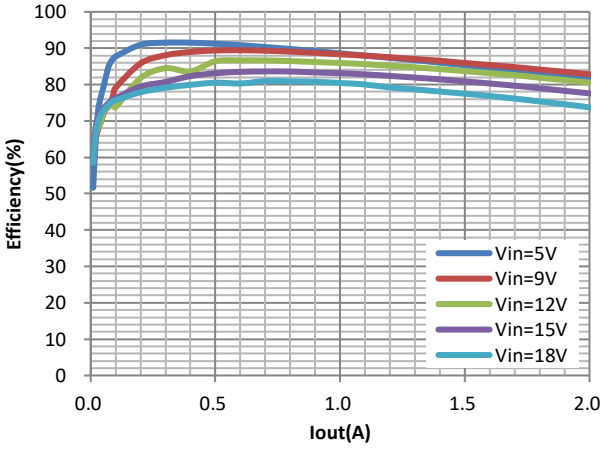
Efficiency vs. Iout
(Vout=1.2V)



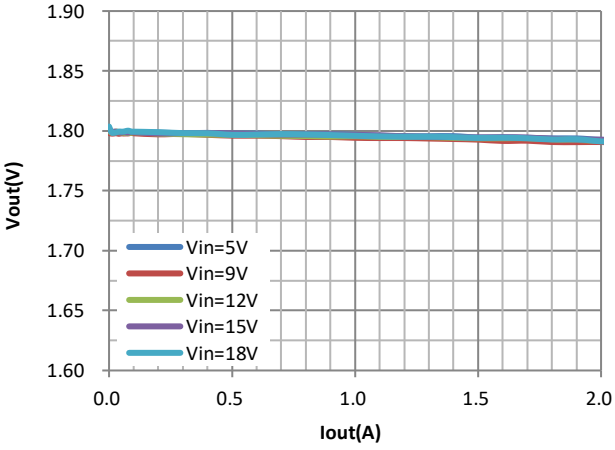
Load Regulation
(Vout=1.2V)



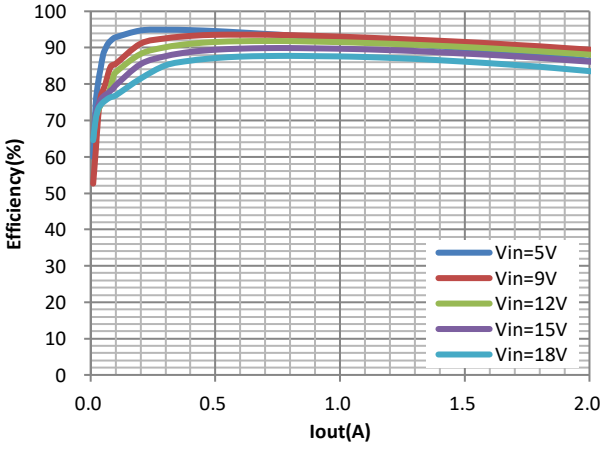
Efficiency vs. Iout
(Vout=1.8V)



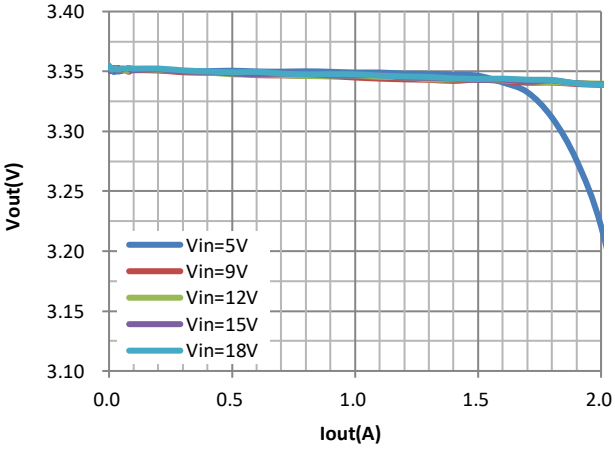
Load Regulation
(Vout=1.8V)



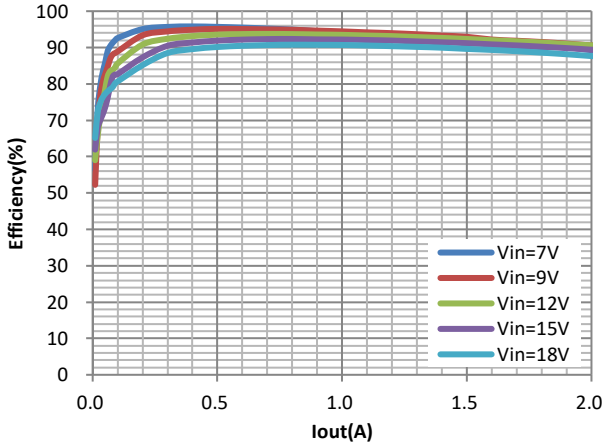
Efficiency vs. Iout
(Vout=3.3V)



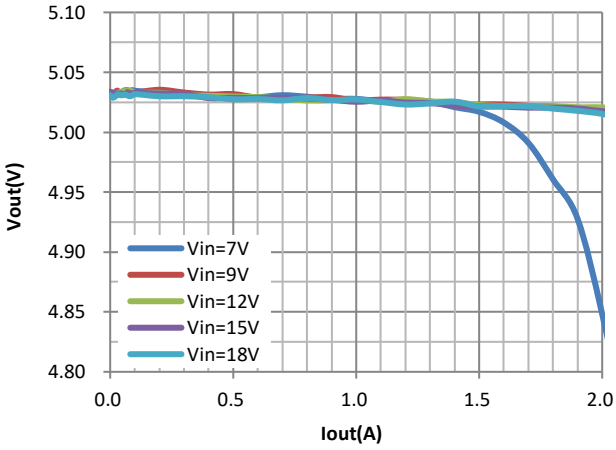
Load Regulation
(Vout=3.3V)



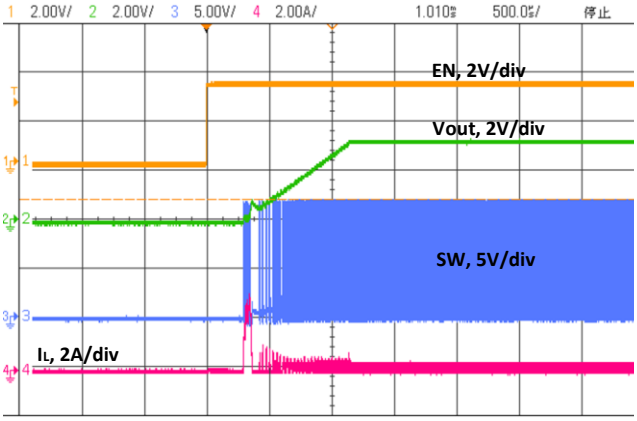
Efficiency vs. Iout
(Vout=5.0V)



Load Regulation
(Vout=5.0V)

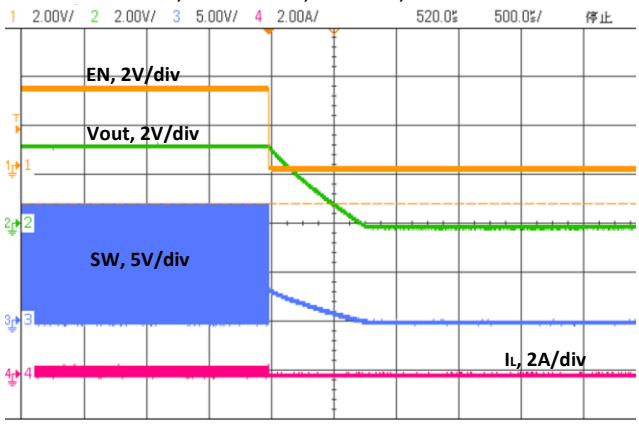


EN Power On
Vin=12V, Vout=3.3V, I_L =0.1A, EN=0V to 3.3V



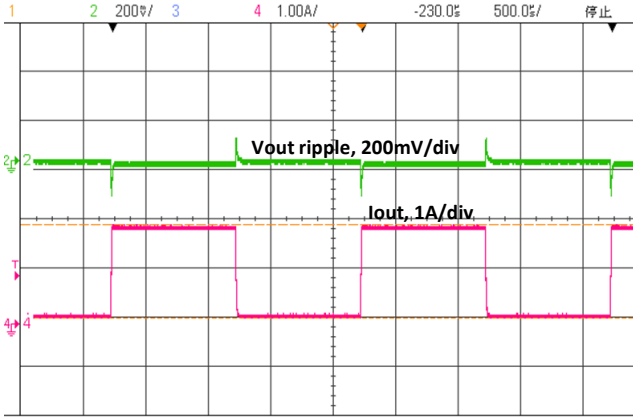
Ch1—EN, Ch2—Vout, Ch3—SW, Ch4—I_L

EN Power Off
Vin=12V, Vout=3.3V, I_L =0.1A, EN=3.3V to 0V



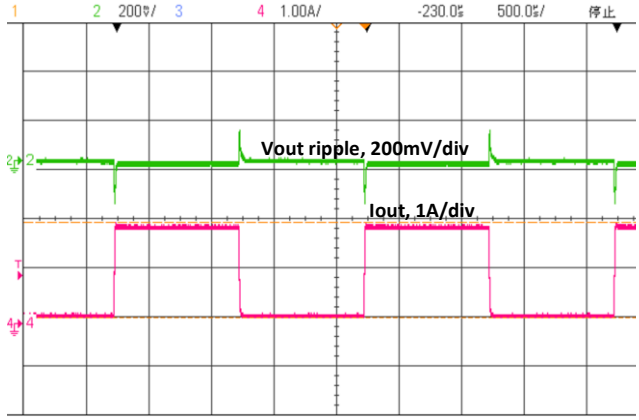
Ch1—EN, Ch2—Vout, Ch3—SW, Ch4—I_L

Load Transient
Vin=12V, Vout=3.3V, Iout=0.2A~2A, R3=0R



Ch2—Vout ripple, Ch4—Iout

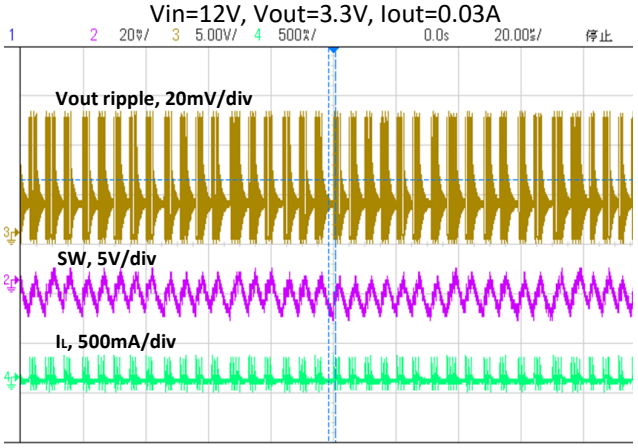
Load Transient
Vin=12V, Vout=3.3V, Iout=0.2A~2A, R3=10KR



Ch2—Vout ripple, Ch4—Iout

Output Ripple Wave

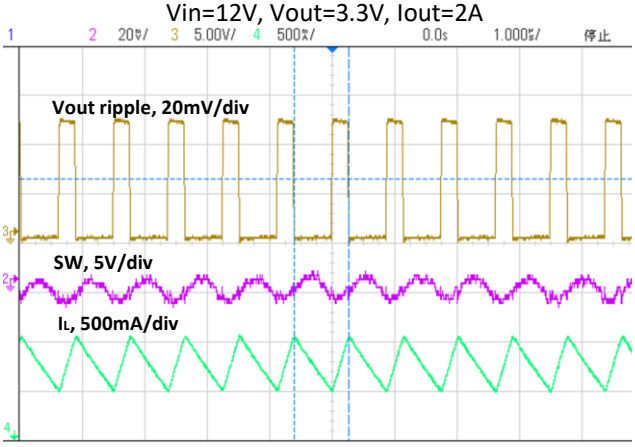
Vin=12V, Vout=3.3V, Iout=0.03A



Ch2—Vout ripple, Ch3—SW, Ch4—I_L

Output Ripple Wave

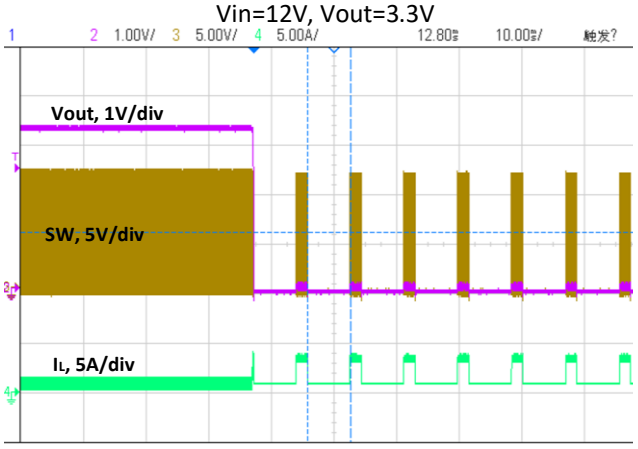
Vin=12V, Vout=3.3V, Iout=2A



Ch2—Vout ripple, Ch3—SW, Ch4—I_L

Short Circuit Protection

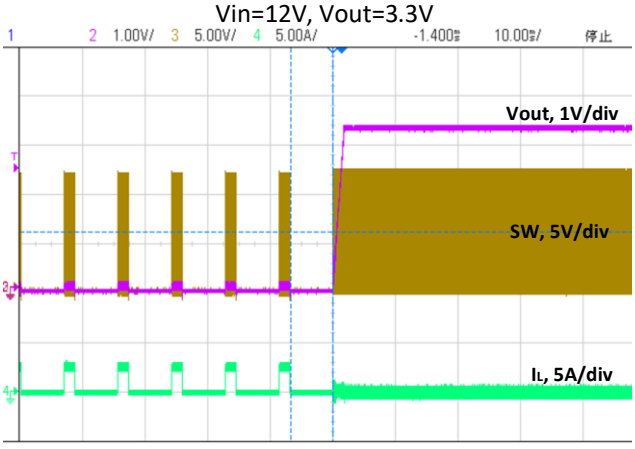
Vin=12V, Vout=3.3V



Ch2—Vout, Ch3—SW, Ch4—I_L

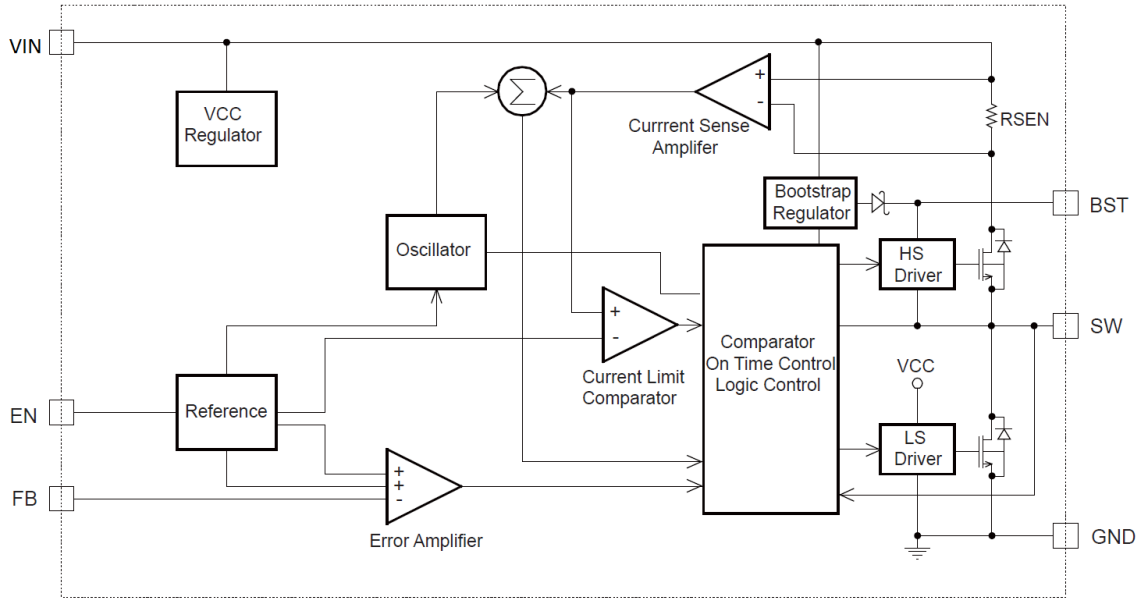
Short Circuit Recovery

Vin=12V, Vout=3.3V



Ch2—Vout, Ch3—SW, Ch4—I_L

BLOCK DIAGRAM



DETAILED DESCRIPTION

Internal Regulator

The BLL2310C is a current mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, and operates at a high 1M operating frequency to ensure a compact, high efficiency design with excellent AC and DC performance.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal FB reference (V_{FB}) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Internal Soft-Start

The soft-start is important for many applications because it eliminates power-up initialization problems. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

Over-Current-Protection and Hiccup

The BLL2310C has a cycle-by-cycle over-current limit for when the inductor current peak value exceeds the set current-limit threshold. First, when the output voltage drops until FB falls below the Short-Voltage threshold (typically 140mV) to trigger a Short circuit event, the BLL2310C enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current to alleviate thermal issues and to protect the regulator. The BLL2310C exits hiccup mode once the overcurrent condition is removed.

Startup and Shutdown

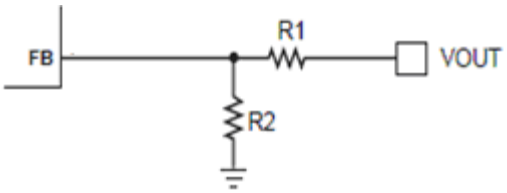
If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATIONS INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 2). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor. R1 and R2 should not be less than the recommended values.

$$R_2 = \frac{R_1}{V_{out}/V_{FB} - 1}$$



Selecting the Inductor

Use a 2.2µH-to-10µH inductor with a DC current rating of at least 25% percent higher than the maximum load current for most applications. For highest efficiency, select an inductor with a DC resistance less than 15mΩ. For most designs, derive the inductance value from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{osc}}$$

Where ΔI_L is the inductor ripple current. Choose an inductor current approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light-load conditions (below 100mA), use a larger inductor to improve efficiency.

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. Use low ESR capacitors to limit the output voltage ripple. Estimate the output voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times \left[R_{ESR} + \frac{1}{8 \times f_S \times C_2}\right]$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, estimate the output voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C_2} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The BLL2310C can be optimized for a wide range of capacitance and ESR values.

PCB LAYOUT

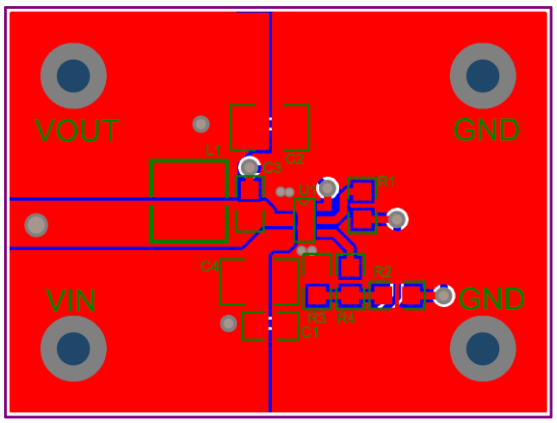
PCB layout is very important to achieve stable operation. For best results, use the following guidelines and figures as reference.

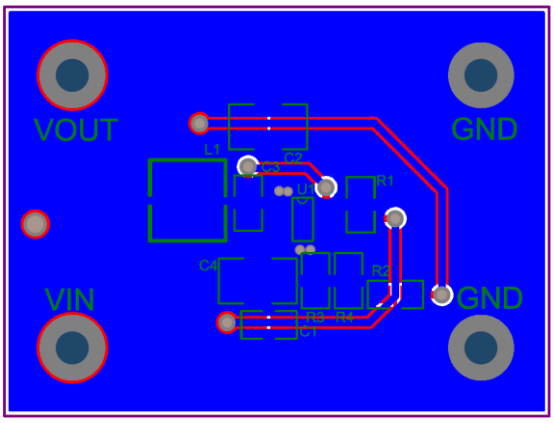
1) Keep the connection between the input ground and GND pin as short and wide as possible.

2) Keep the connection between the input capacitor and VIN pin as short and wide as possible.

3) Use short and direct feedback connections. Place the feedback resistors and compensation components as close to the chip as possible.

4) Route SW away from sensitive analog areas such as FB.

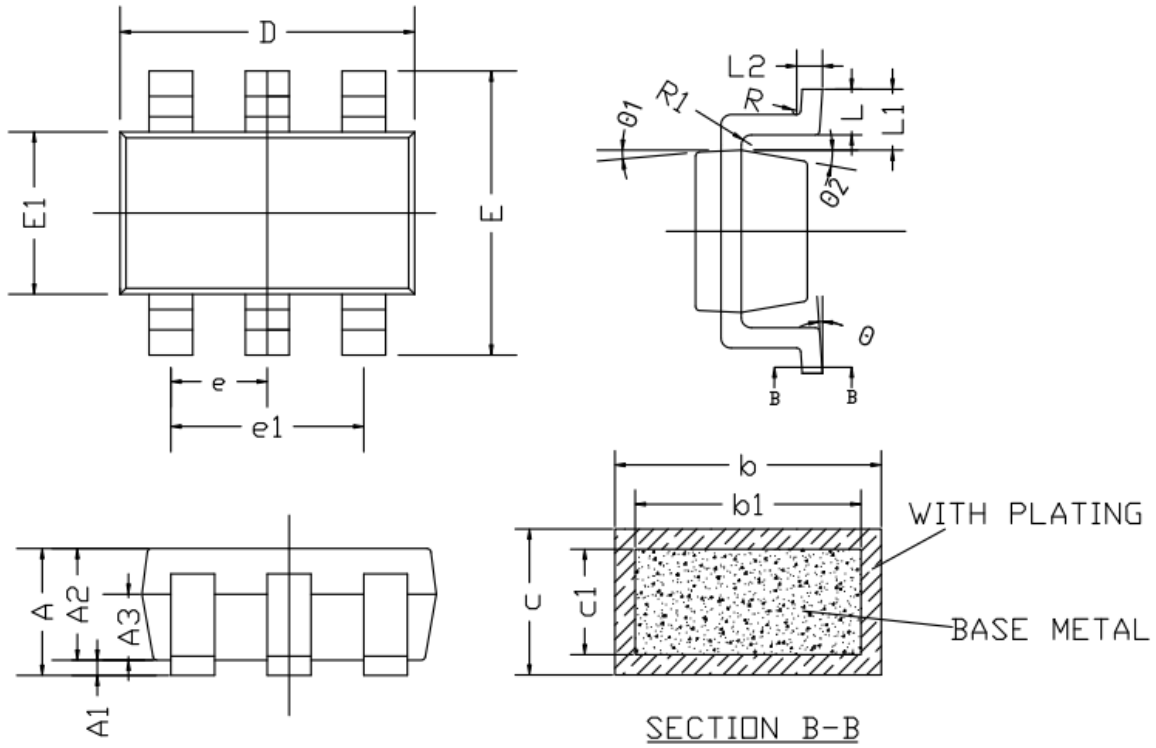




PACKAGE OUTLINE

Package	SOT23-6	Devices per reel	3000pcs	Vendor	QingDao TRS Microelectronics Co., Ltd

Package dimension:



COMMON DIMENSION (MM)				DIMENSION In Inches		
PKG	SOT23-6L			SOT23-6L		
REF.	MIN.	NOM.	MAX	MIN.	NOM.	MAX
A	–	–	1.250	–	–	0.049
A1	0.000	–	0.150	0.000	–	0.006
A2	1.000	1.100	1.200	0.039	0.043	0.047
A3	0.600	0.650	0.700	0.024	0.026	0.028
b	0.300	–	0.450	0.012	–	0.018
b1	0.300	0.350	0.400	0.012	0.014	0.016
c	0.140	–	0.200	0.006	–	0.008
c1	0.140	0.150	0.160	0.006	0.006	0.006
D	2.826	2.926	3.026	0.111	0.115	0.119
E	2.600	2.800	3.000	0.102	0.110	0.118
E1	1.526	1.626	1.726	0.060	0.064	0.068
e	0.900	0.950	1.000	0.035	0.037	0.039
e1	1.800	1.900	2.000	0.071	0.075	0.079
L	0.350	0.450	0.600	0.014	0.018	0.024
L1		0.590REF			0.023REF	
L2		0.250BSC			0.010BSC	
R	0.050	–	–	0.002	–	–
R1	0.050	–	0.200	0.002	–	0.008
θ	0°	–	8°	0°	–	8°
θ1	3°	5°	7°	3°	5°	7°
θ2	6°	–	14°	6°	–	14°