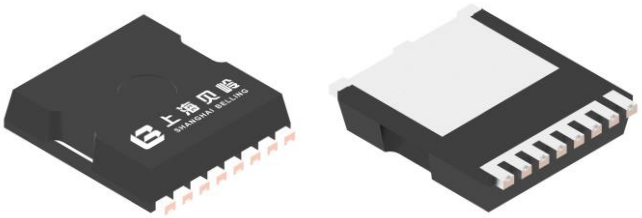
40V MOSFET BLP01N04

1. Product Features

- Fast Switching
- Low On-Resistance
- Low Gate Charge
- Low Reverse transfer capacitances
- High avalanche ruggedness
- RoHS product



TOLL8

Key characteristics

Parameter	Value	Unit
V_{DSS}	40	V
I_D	330	A
$R_{DS(on)@10V.typ}$	1.05	mΩ

2. Product Applications

- Synchronous rectification
- High speed switching applications

3. Description

BLP01N04, the N-channel Enhanced Power MOSFETs, is obtained by advanced **double trench** technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. This is suitable device for synchronous rectification and high speed switching applications.

4. Ordering Guide

Product Number	Package	Operating Temp.	Eco Status	MSL	Minimum Pack Qty
BLP01N04-T	TOLL8	-55~175°C	Green	3	1200/Reel

Contents

5. Pin Description

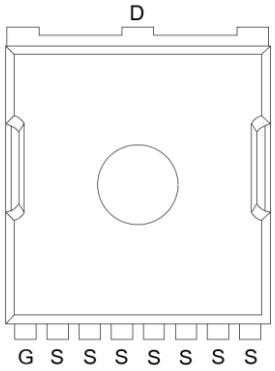


Fig 1 Pin Description

6. Specifications

6.1 Absolute Ratings

At T_C = 25°C, unless otherwise specified.

Table 1 Absolute Ratings

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-Source Voltage	40	V
I_D	Continuous Drain Current, Silicon Limited	330	A
	Continuous Drain Current @T_C=100°C, Silicon Limited	233.3	A
I_{DM} Note1	Pulsed Drain Current	1320	A
V_{GS}	Gate-Source Voltage	±20	V
E_{AS} Note2	Avalanche Energy	702	mJ
P_D	Power Dissipation	230.7	W
	Derating Factor above 25°C	1.54	W/°C
T_J，T_{stg}	Operating Junction and Storage Temperature Range	–55 to 175	°C
T_L	Maximum Temperature for Soldering	260	°C

Note1：Repetitive Rating：Pulse width limited by maximum junction temperature

Note2：L=0.5mH, Ias=53A, Start T_J = 25°C

6.2 Thermal Characteristics

Table 2 Thermal Characteristics

Symbol	Parameter	Max	Units
$R_{\theta JC}$	thermal resistance, Junction-Case	0.65	°C/W
$R_{\theta JA}$	thermal resistance, Junction-Ambient	75	°C/W

6.3 Electrical Characteristics

At T_C = 25°C, unless otherwise specified.

6.3.1 OFF Characteristics

Table 3 OFF Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40	--	--	V
I_{DSS}	Drain-Source Leakage Current	V_{DS}=40V, V_{GS}=0V	--	--	1	μA
		V_{DS}=32V, V_{GS}=0V @T_C=125°C	--	--	100	μA
$I_{GSS(F)}$	Gate-Source Forward Leakage	V_{GS}=+20V	--	--	100	nA
$I_{GSS(R)}$	Gate-Source Reverse Leakage	V_{GS}=-20V	--	--	-100	nA

6.3.2 ON Characteristics

Table 4 ON Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=50A	--	1.05	1.3	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2.2	2.6	3	V

Pulse width tp≤300μs, δ≤2%

6.3.3 Dynamic Characteristics

Table 5 Dynamic Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
Ciss	Input Capacitance	V_{DS}=20V, V_{GS}=0, f=0.1MHz	--	10062	--	pF
Coss	Output Capacitance		--	3886	--	
Crss	Reverse Transfer Capacitance		--	52	--	
Q_g	Total Gate Charge	V_{DD}=20V, I_D=50A, V_{GS}=10V	--	111	--	nC
Q_{gs}	Gate-Source charge		--	39.3	--	
Q_{gd}	Gate-Drain charge		--	7	--	

6.3.4 Switching Characteristics

Table 6 Switching Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=20V, V_{GS}=10V, R_G=5Ω, Resistive Load	--	61	--	ns
t_r	Rise Time		--	30	--	
$t_{d(off)}$	Turn-Off Delay Time		--	137	--	
t_f	Fall Time		--	35	--	

6.3.5 Source-Drain Diode Characteristics

Table 7 Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current		--	--	330	A
I_{SM}	Maximum Pulsed Current		--	--	1320	A
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_S=50A	0.5	--	1.2	V
T_{rr}	Reverse Recovery Time	I_S=50A, V_{GS}=0, di/dt=100A/us	--	77	--	ns
Q_{rr}	Reverse Recovery Charge		--	90	--	nC

6.4 Characteristics Curves

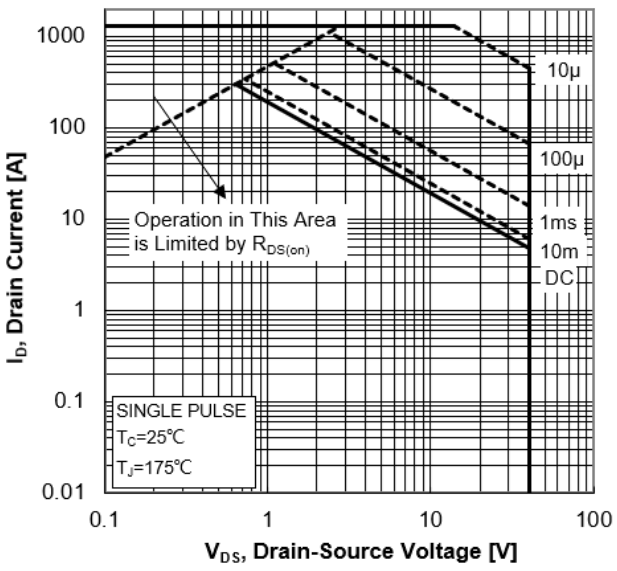


Figure 2 Safe Operating Area

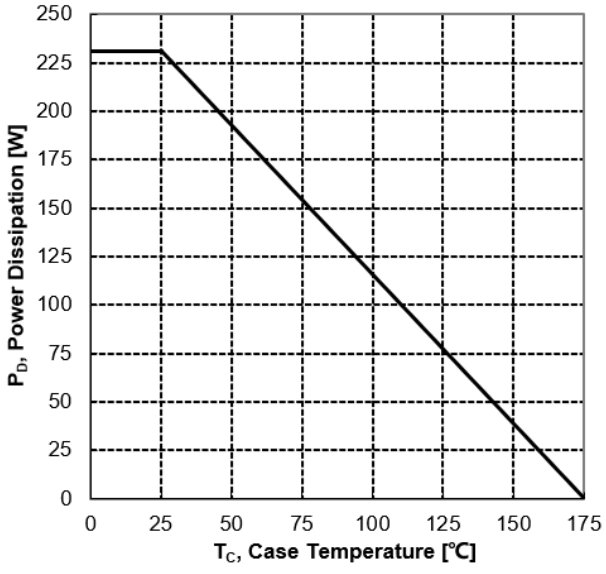


Figure 3 Maximum Power Dissipation vs Case Temperature

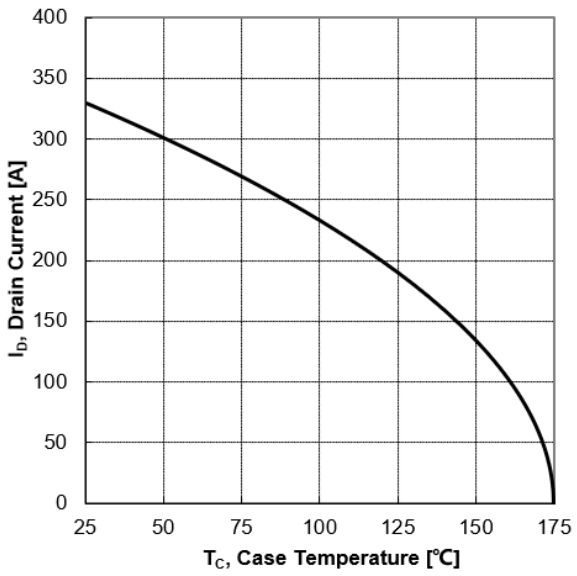


Figure 4 Maximum Continuous Drain Current vs Case Temperature

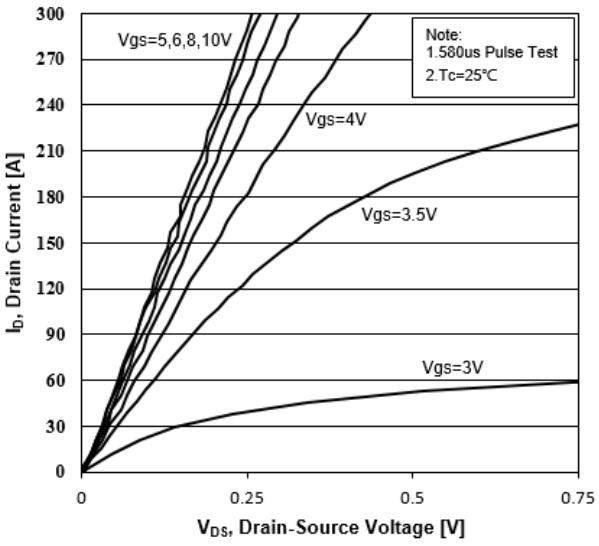


Figure 5 Typical Output Characteristics

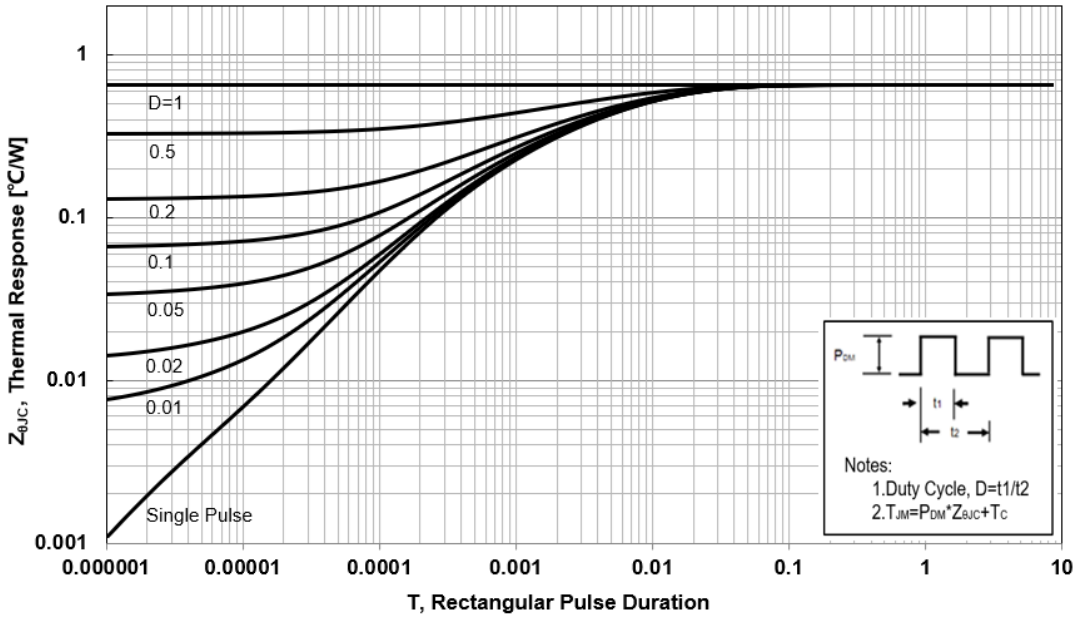


Figure 6 Transient Thermal Impedance

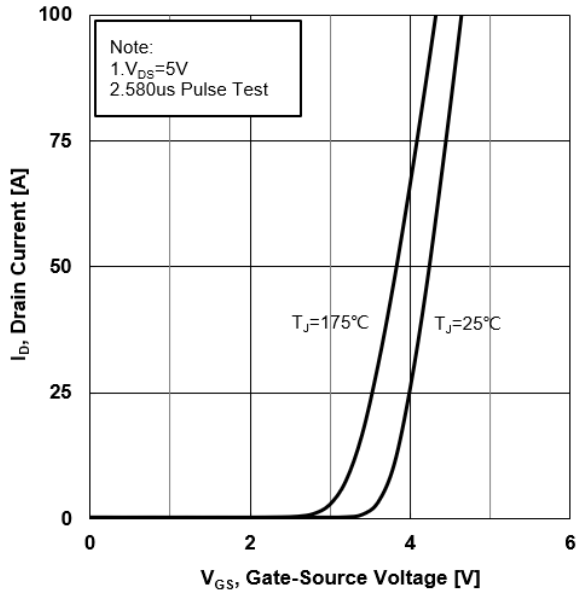


Figure 7 Typical Transfer Characteristics

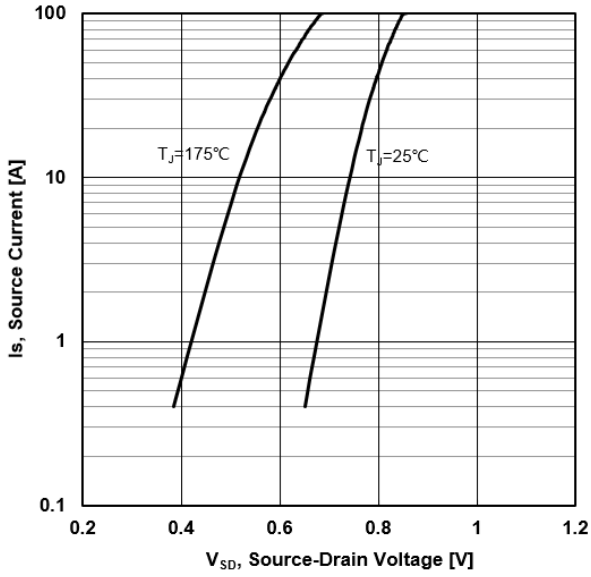


Figure 8 Source-Drain Diode Forward Characteristics

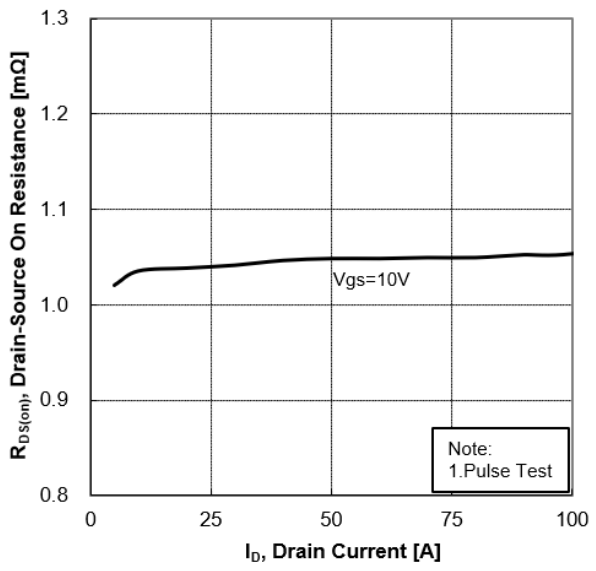


Figure 9 Drain-Source On-Resistance vs Drain Current

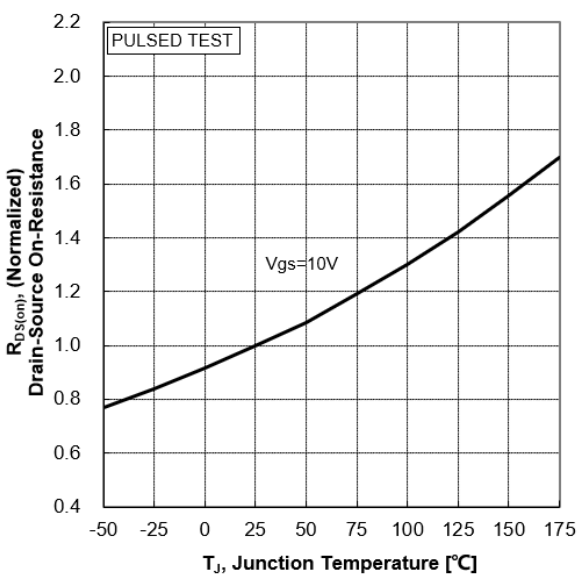


Figure 10 Normalized On-Resistance vs Junction Temperature

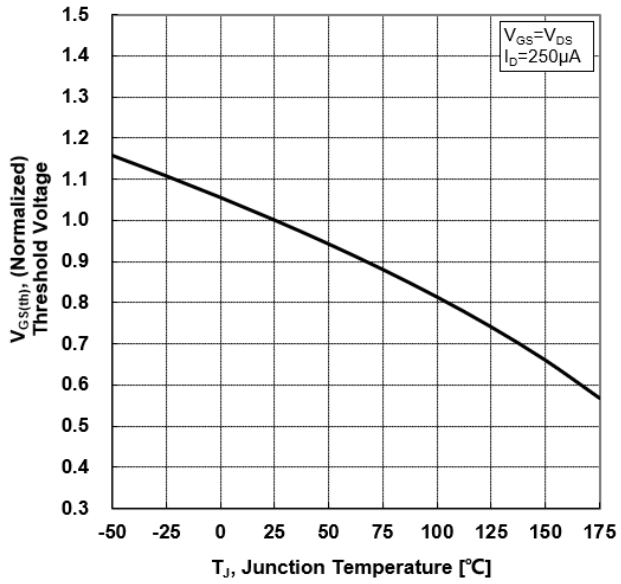


Figure 11 Normalized Threshold Voltage vs Junction Temperature

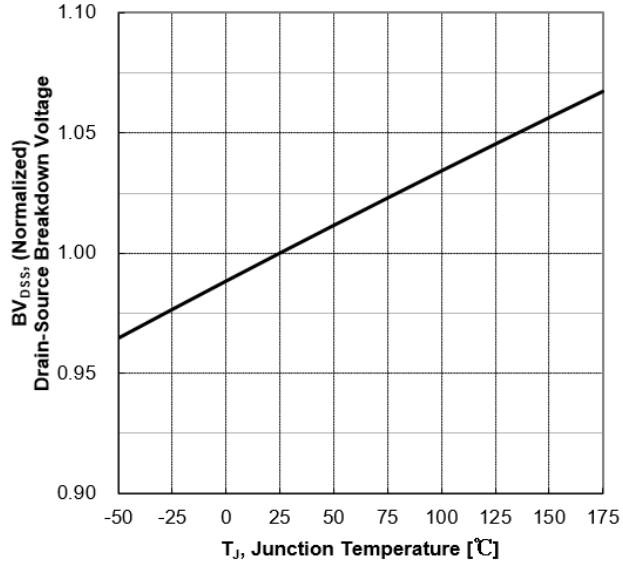


Figure 12 Normalized Breakdown Voltage vs Junction Temperature

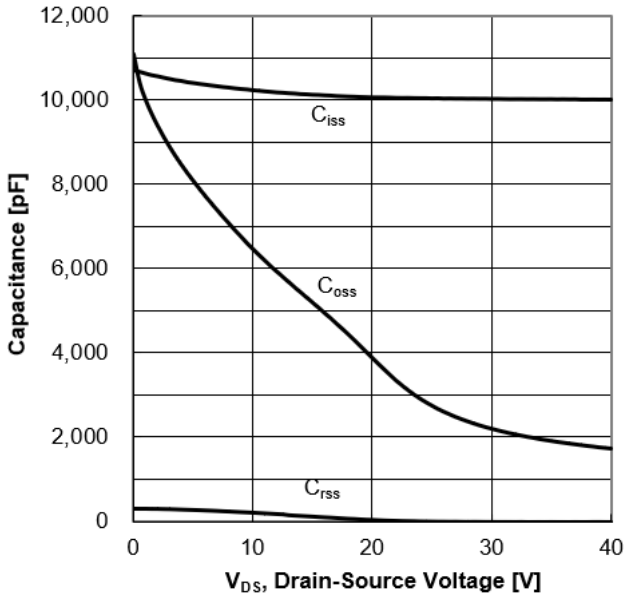


Figure 13 Capacitance Characteristics

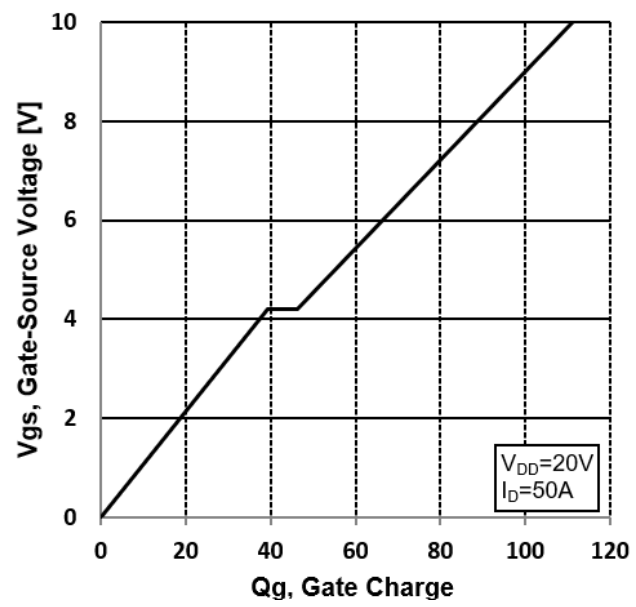


Figure 14 Typical Gate Charge vs Gate-Source Voltage

7. Detailed Description

7.1 Test Circuit and Waveform

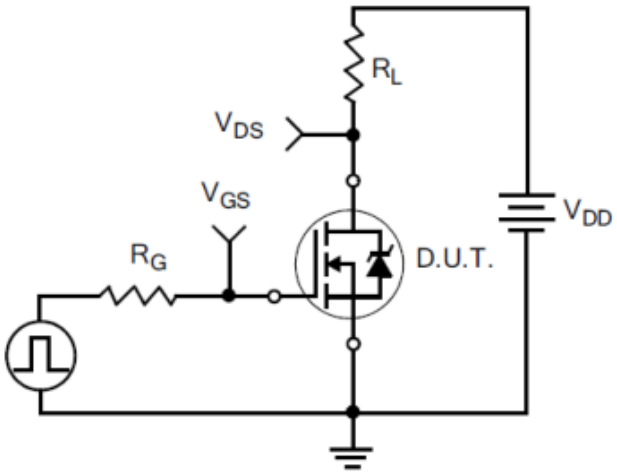


Figure 15 Resistive Switching Test Circuit

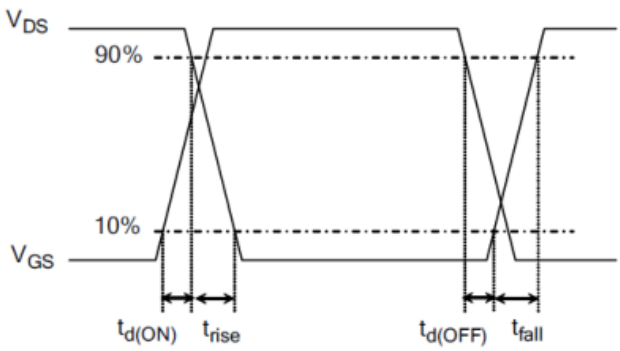


Figure 16 Resistive Switching Waveforms

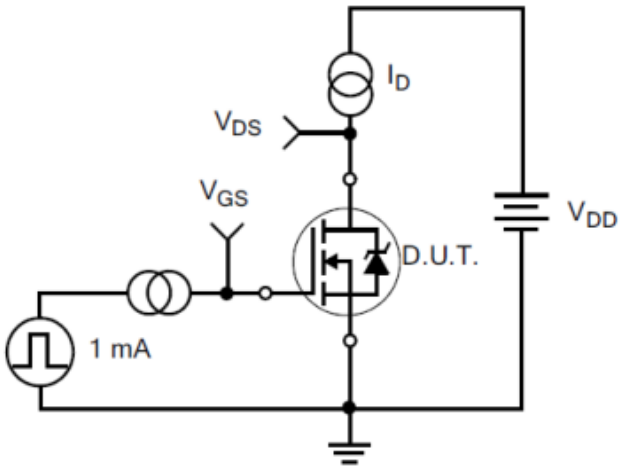


Figure 17 Gate Charge Test Circuit

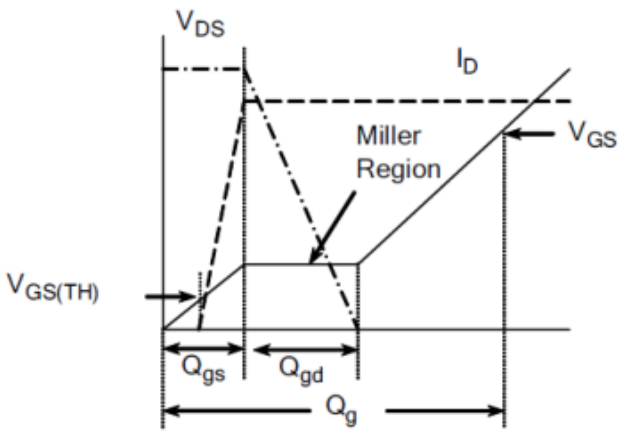


Figure 18 Gate Charge Waveforms

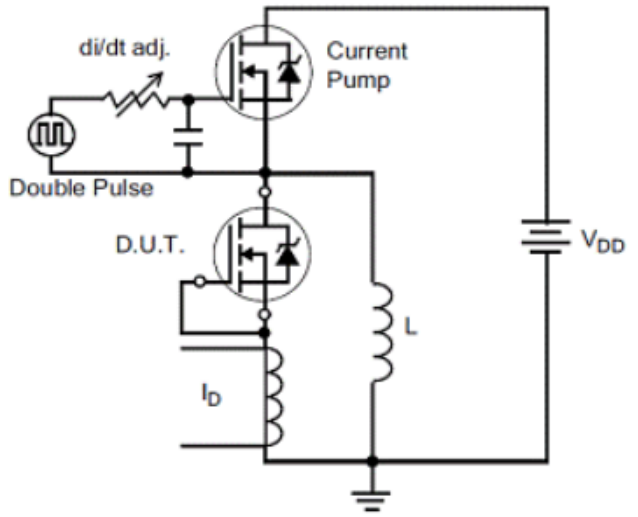


Figure 19 Diode Reverse Recovery Test Circuit

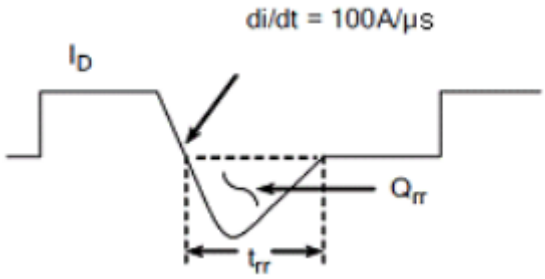


Figure 20 Diode Reverse Recovery Waveform

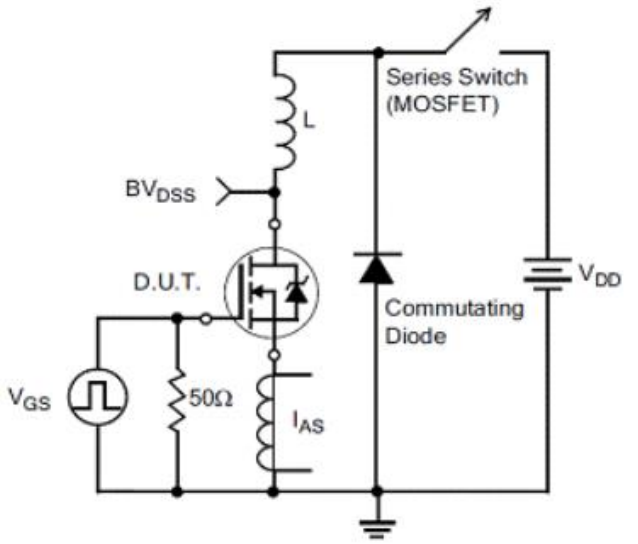


Figure 21 Unclamped Inductive Switching Test Circuit

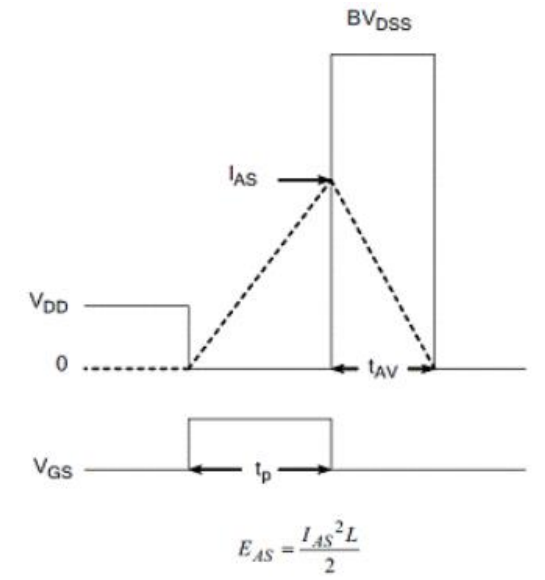
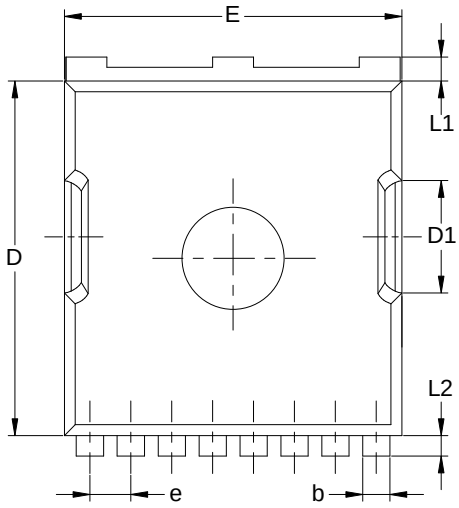


Figure 22 Unclamped Inductive Switching Waveform

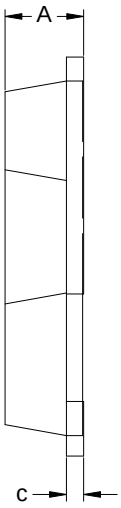
8. Package Information

8.1 Package Outline Dimensions

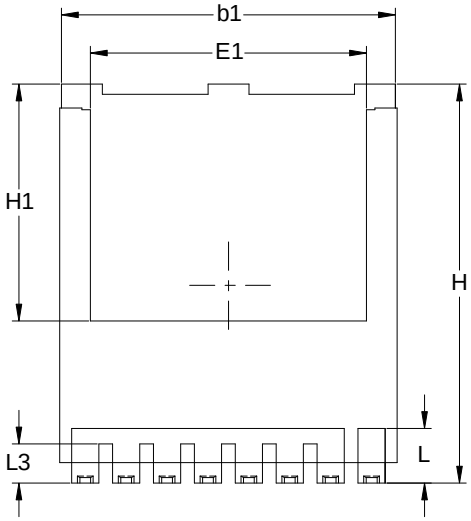
8.1.1 TOLL8



TOP VIEW



SIDE VIEW

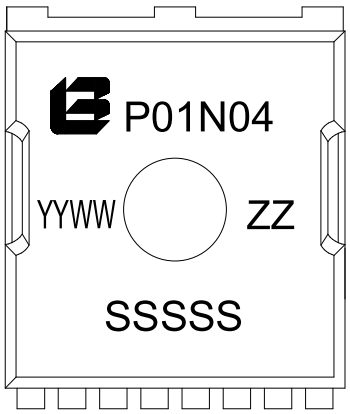


BOTTOM VIEW

SIDE VIEW

COMMON DIMENSION&TOLERANCE			
SYMBOL	ALL DIMENSION IN MILLIMETERS		
	MIN	MON	MAX
A	2.15	2.30	2.45
b	0.60	---	0.90
b1	9.65	9.80	9.95
c	0.35	0.50	0.65
D	10.18	---	10.70
D1	3.15	3.30	3.45
E	9.70	9.90	10.10
E1	7.90	---	9.05
e	1.20 BSC		
H	11.45	11.70	11.95
H1	6.75	---	7.50
L	1.35	---	2.10
L1	0.50	0.70	0.90
L2	0.40	0.60	0.80
L3	0.90	---	1.35

8.2 Marking



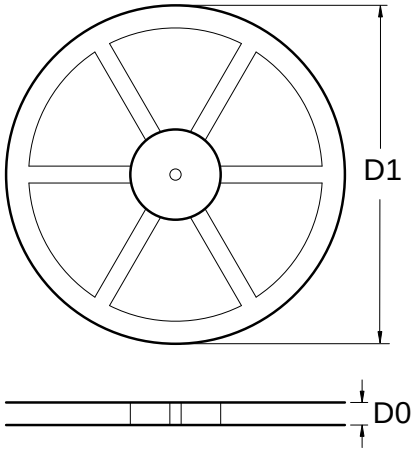
Marking Drawing

Content	Note
P01N04	Device Mark
YY	Calendar year code
WW	Workweek date code
ZZ	Assembly factory code
SSSSS	Lot ID

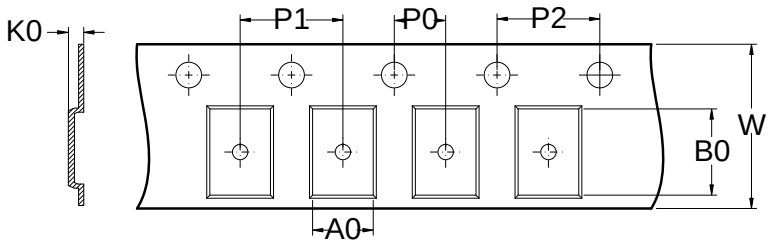
9. Packing specifications

9.1 TOLL8 Reel Package

REEL DIMENSIONS

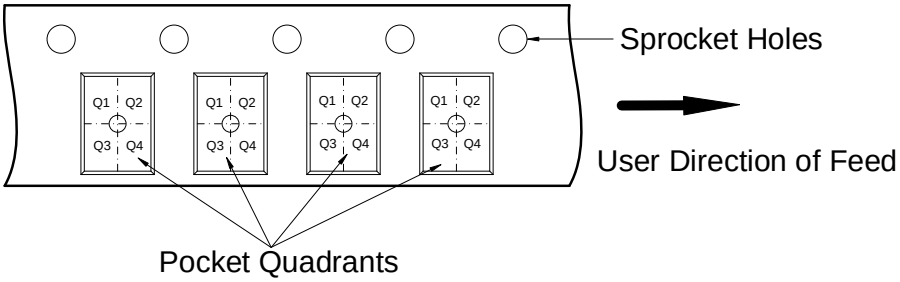


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W： Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

*All dimensions are nominal

Device	Package Type	Pins	SPQ	D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
BLPXXXX	TOLL8	8	1200	330	24.5	10.30	12.10	2.65	2	12	4	24	Q3

Revision History

Revision	Date	Changes
Version 01	2026-04	Initial Version

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