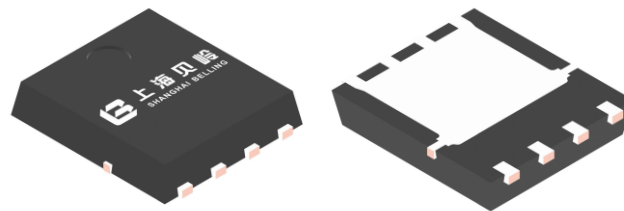


40V MOSFET BLP01N04LC

1. Product Features

- Fast Switching
- Low On-Resistance
- Low Gate Charge
- Low Reverse transfer capacitances
- High avalanche ruggedness
- RoHS product



PDFN 5*6-8L

Key characteristics

Parameter	Value	Unit
V_{DS}	40	V
I_D	315	A
$R_{DS(on)}@4.5V_{typ}$	1.05	mΩ
$R_{DS(on)}@10V_{typ}$	0.75	mΩ

2. Product Applications

- Synchronous rectification
- High speed switching applications

3. Description

BLP01N04LC, the N-channel Enhanced Power MOSFETs, is obtained by advanced **double trench** technology **Cu clip bond** Assembly technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. This is suitable device for synchronous rectification and high speed switching applications.

4. Ordering Guide

Product Number	Package	Operating Temp.	Eco Status	MSL	Minimum Pack Qty
BLP01N04LC-Q	PDFN 5*6-8L	-55~175°C	Green	3	5000/Reel

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5. Pin Description

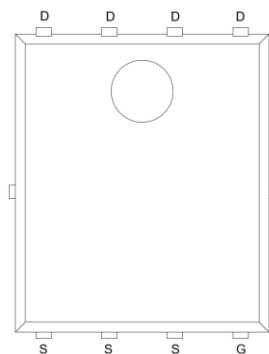


Fig 1 Pin Description

6. Specifications

6.1 Absolute Ratings

At $T_C = 25^\circ\text{C}$, unless otherwise specified.

Table 1 Absolute Ratings

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-Source Voltage	40	V
I_D	Continuous Drain Current, Silicon Limited	315	A
	Continuous Drain Current @ $T_C=100^\circ\text{C}$, Silicon Limited	222.7	A
I_{DM} Note1	Pulsed Drain Current	1260	A
V_{GS}	Gate-Source Voltage	± 20	V
E_{AS} Note2	Avalanche Energy	900	mJ
P_D	Power Dissipation	186.5	W
	Derating Factor above 25°C	1.24	W/ $^\circ\text{C}$
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to 175	$^\circ\text{C}$
T_L	Maximum Temperature for Soldering	260	$^\circ\text{C}$

Note1: Repetitive Rating: Pulse width limited by maximum junction temperature

Note2: $L=0.5\text{mH}$, $I_{as}=60\text{A}$, Start $T_J = 25^\circ\text{C}$

6.2 Thermal Characteristics

Table 2 Thermal Characteristics

Symbol	Parameter	Max	Units
$R_{\theta JC}$	thermal resistance, Junction-Case	0.8	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	thermal resistance, Junction-Ambient	75	$^\circ\text{C}/\text{W}$

6.3 Electrical Characteristics

At $T_C = 25^\circ\text{C}$, unless otherwise specified.

6.3.1 OFF Characteristics

Table 3 OFF Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	--	--	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=40V, V_{GS}=0V$	--	--	1	μA
		$V_{DS}=32V, V_{GS}=0V$ @ $T_C=125^\circ\text{C}$	--	--	100	μA
$I_{GSS(F)}$	Gate-Source Forward Leakage	$V_{GS}=+20V$	--	--	100	nA
$I_{GSS(R)}$	Gate-Source Reverse Leakage	$V_{GS}=-20V$	--	--	-100	nA

6.3.2 ON Characteristics

Table 4 ON Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
$R_{DS(on)}$	Drain-Source On-Resistance	$V_{GS}=4.5V, I_D=20A$	--	1.05	1.5	$m\Omega$
		$V_{GS}=10V, I_D=50A$	--	0.75	1	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.7	2.5	V

Pulse width $t_p \leq 300\mu s$, $\delta \leq 2\%$

6.3.3 Dynamic Characteristics

Table 5 Dynamic Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	$V_{DS}=20V,$ $V_{GS}=0,$ $f=0.1MHz$	--	7978	--	pF
C_{oss}	Output Capacitance		--	4705	--	
C_{rss}	Reverse Transfer Capacitance		--	245	--	
Q_g	Total Gate Charge	$V_{DD}=20V,$ $I_D=50A,$ $V_{GS}=10V$	--	131.5	--	nC
Q_{gs}	Gate-Source charge		--	24.1	--	
Q_{gd}	Gate-Drain charge		--	18.5	--	

6.3.4 Switching Characteristics

Table 6 Switching Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
$t_{d(on)}$	Turn-On Delay Time	$V_{DD}=20V$, $V_{GS}=10V$, $R_G=3\Omega$, Resistive Load	--	31	--	ns
t_r	Rise Time		--	70	--	
$t_{d(off)}$	Turn-Off Delay Time		--	95	--	
t_f	Fall Time		--	29	--	

6.3.5 Source-Drain Diode Characteristics

Table 7 Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current		--	--	315	A
I_{SM}	Maximum Pulsed Current		--	--	1260	A
V_{SD}	Diode Forward Voltage	$V_{GS}=0V$, $I_S=50A$	0.5	--	1.2	V
T_{rr}	Reverse Recovery Time	$I_S=50A$, $V_{GS}=0$,	--	79	--	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=100A/us$	--	108	--	nC

6.4 Characteristics Curves

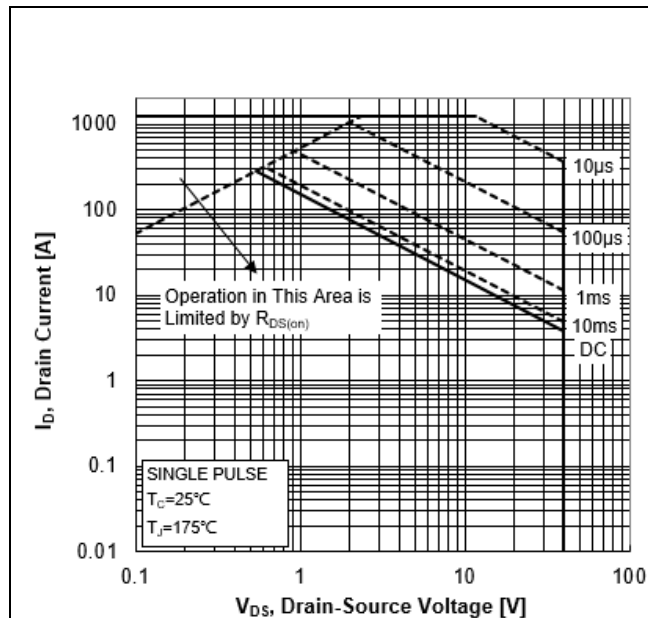


Figure 2 Safe Operating Area

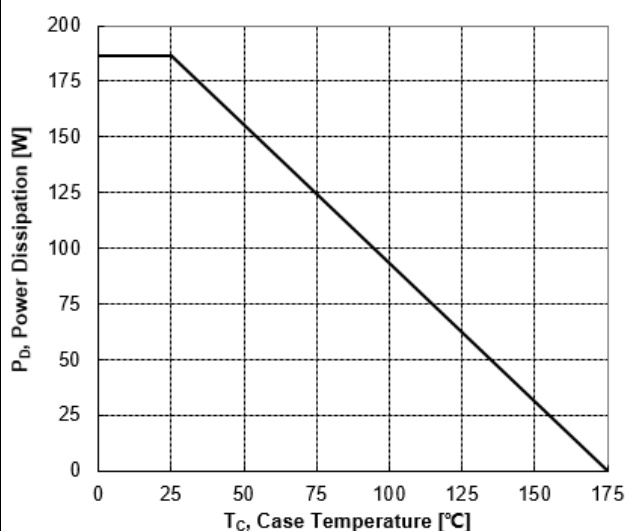


Figure 3 Maximum Power Dissipation vs Case Temperature

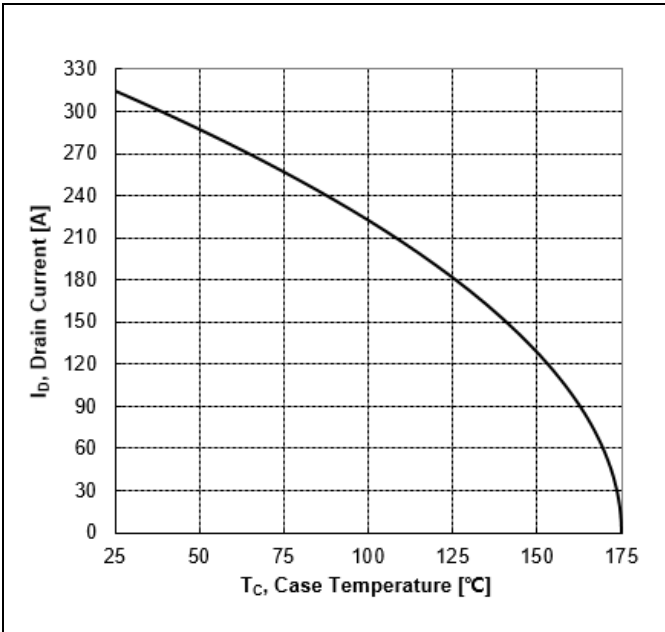


Figure 4 Maximum Continuous Drain Current vs Case Temperature

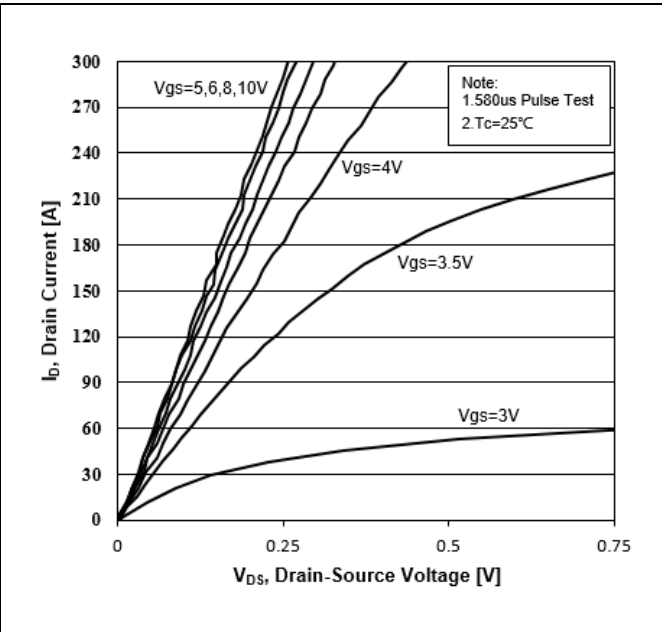


Figure 5 Typical Output Characteristics

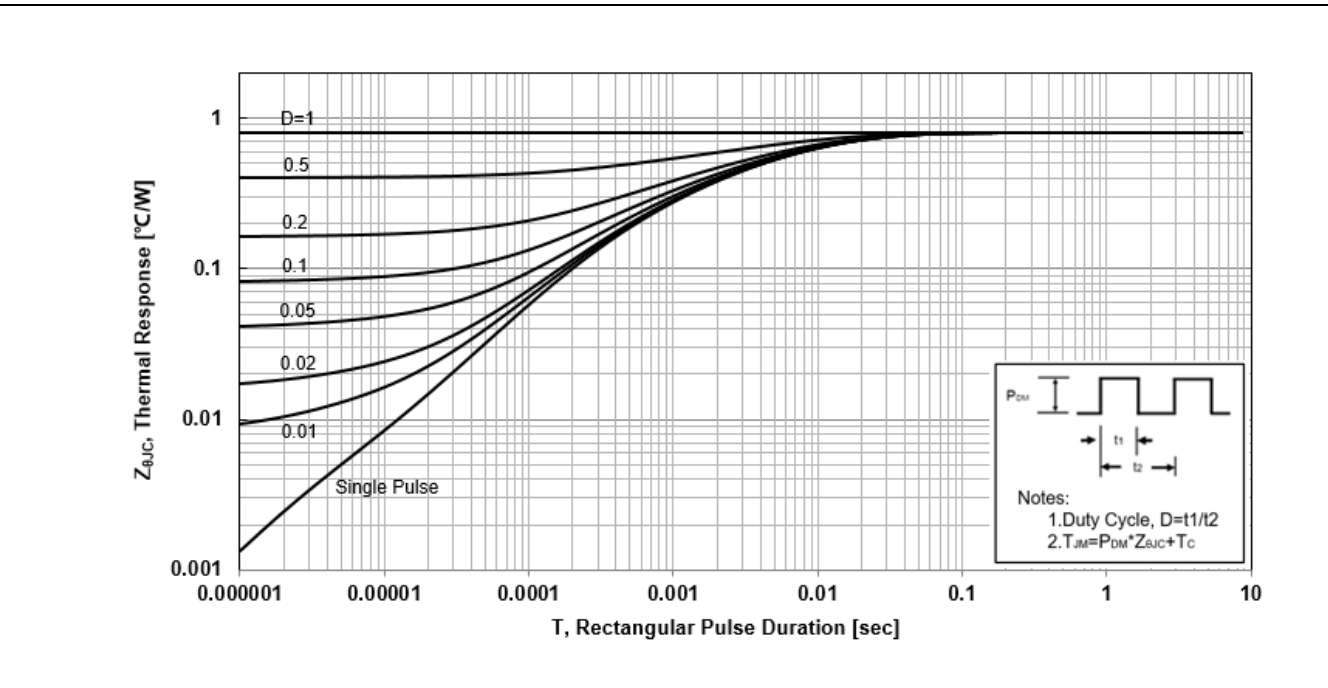


Figure 6 Transient Thermal Impedance

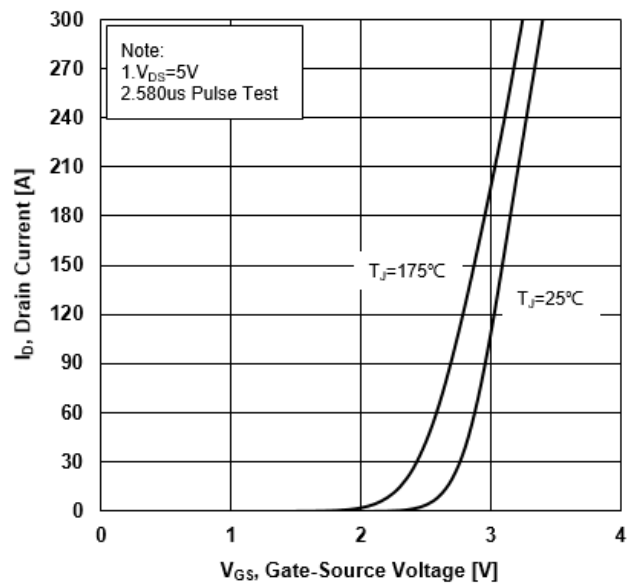


Figure 7 Typical Transfer Characteristics

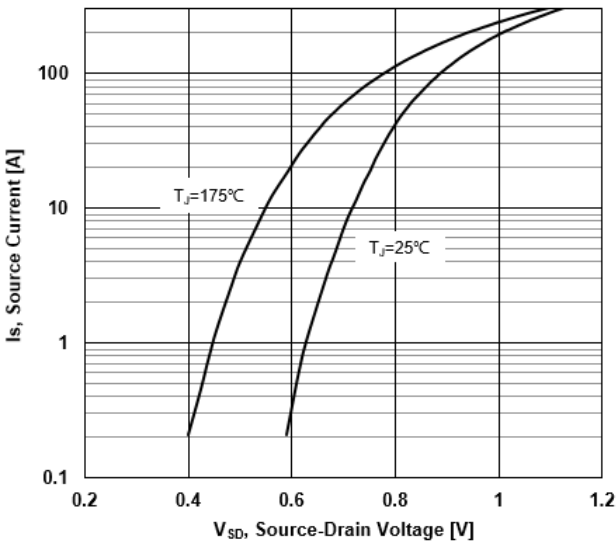


Figure 8 Source-Drain Diode Forward Characteristics

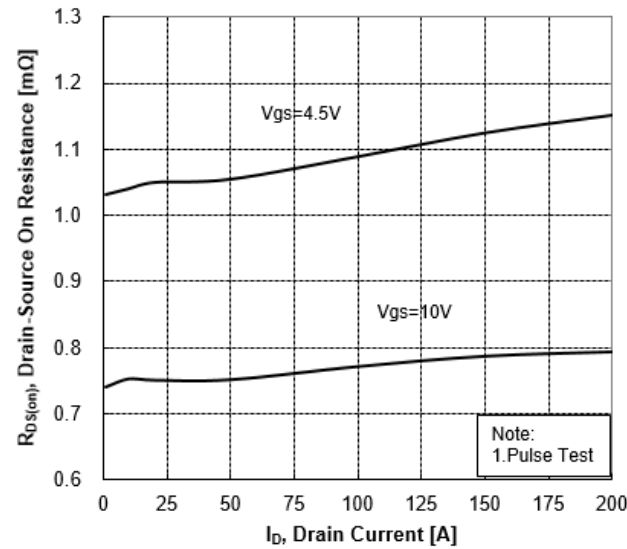


Figure 9 Drain-Source On-Resistance vs Drain Current

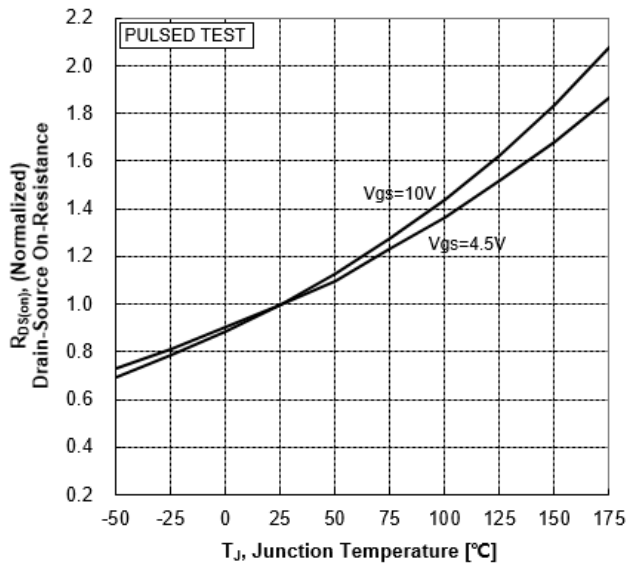


Figure 10 Normalized On-Resistance vs Junction Temperature

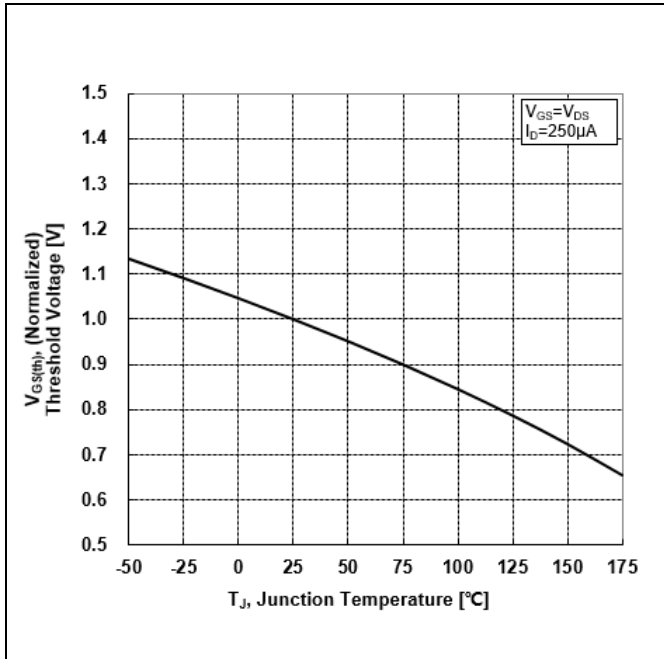


Figure 11 Normalized Threshold Voltage vs Junction Temperature

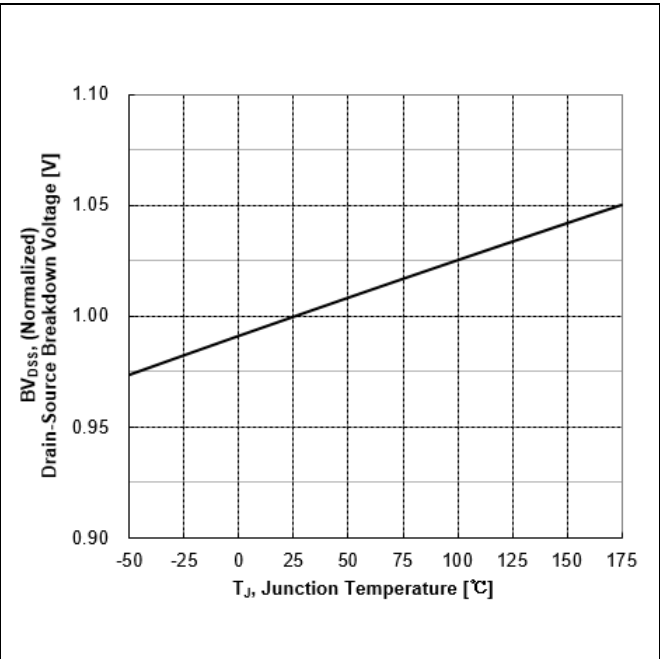


Figure 12 Normalized Breakdown Voltage vs Junction Temperature

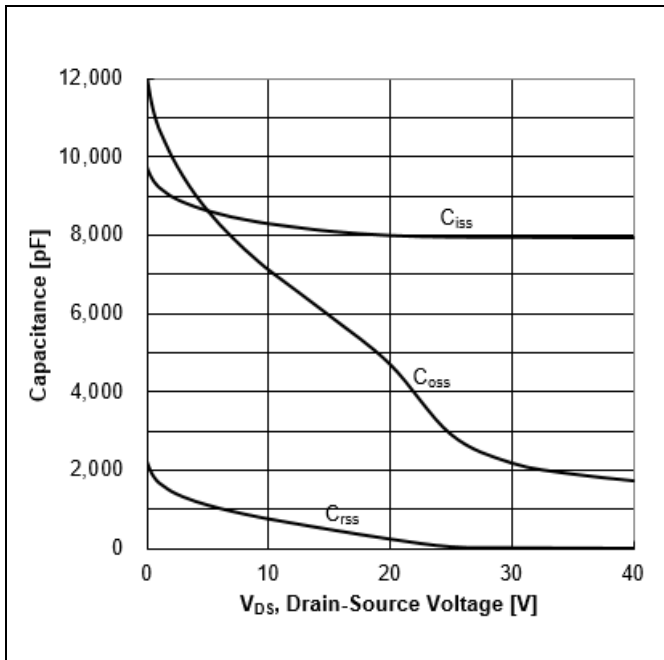


Figure 13 Capacitance Characteristics

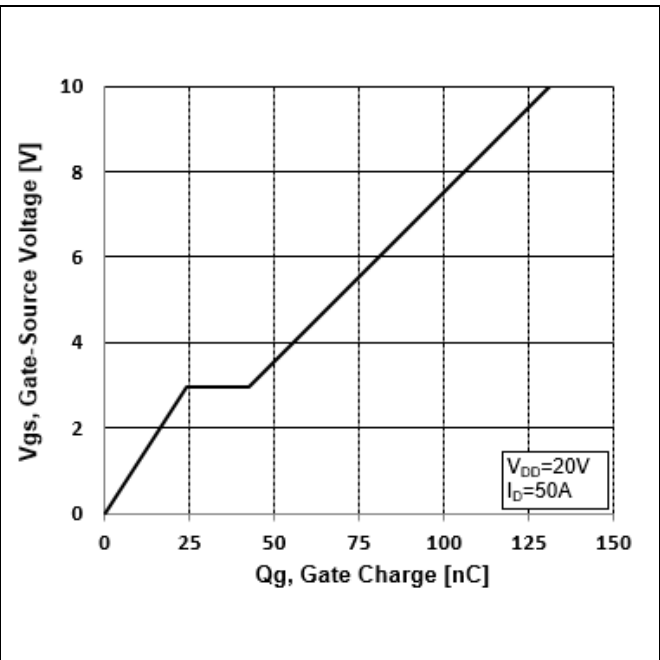
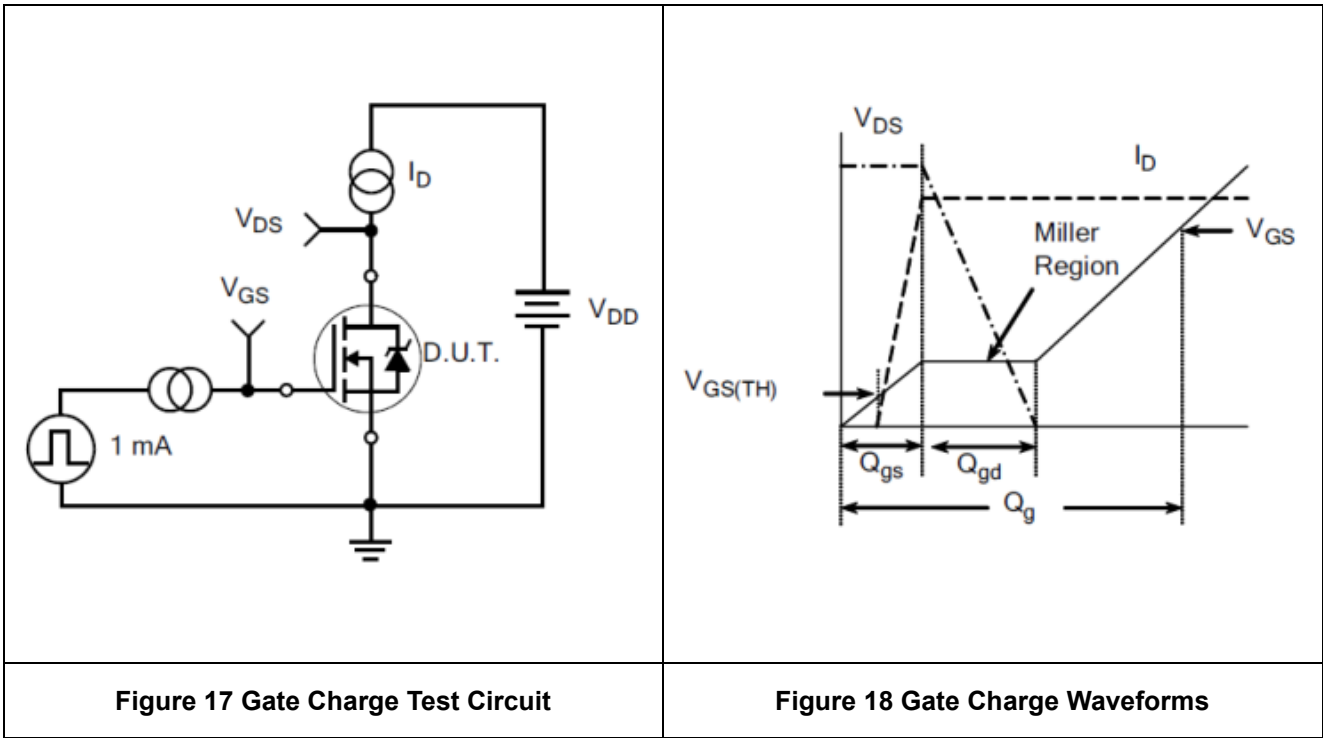
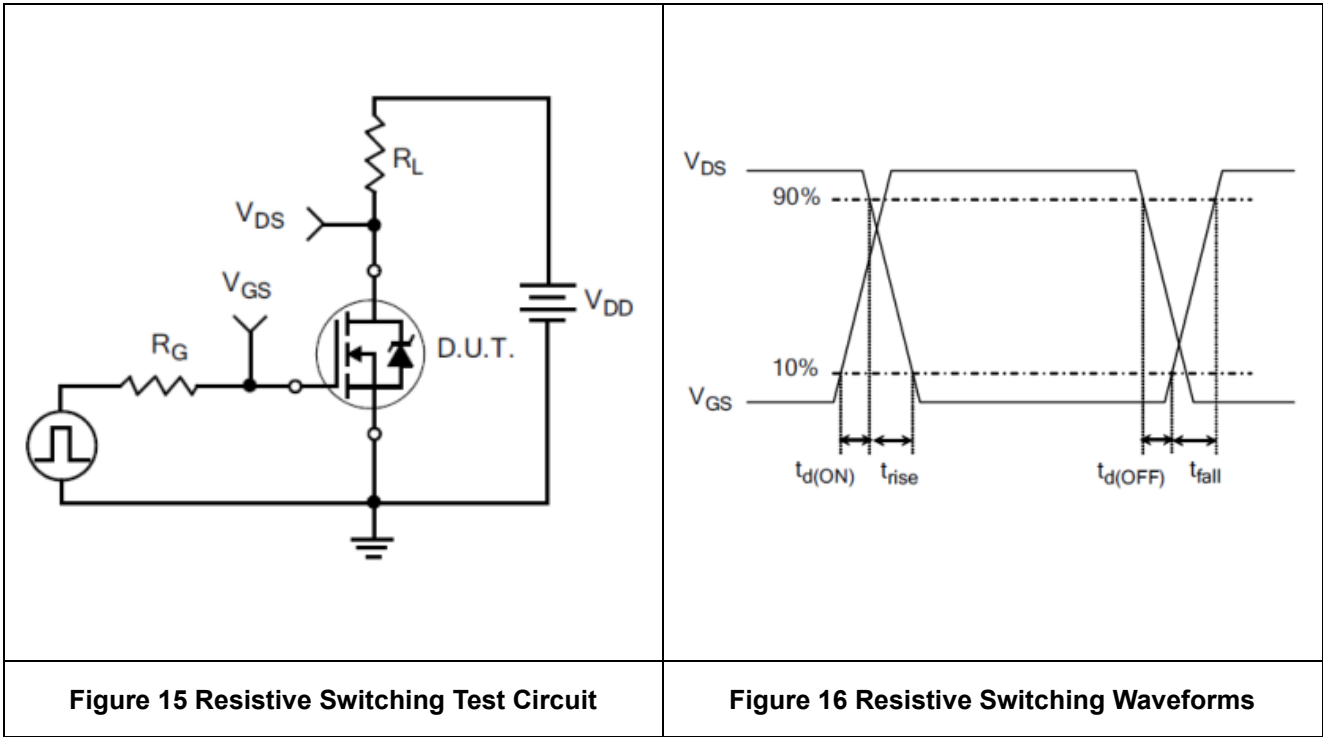


Figure 14 Typical Gate Charge vs Gate-Source Voltage

7. Detailed Description

7.1 Test Circuit and Waveform



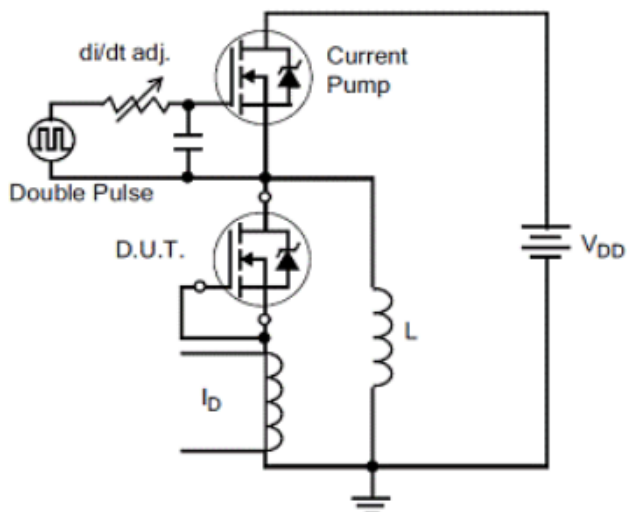


Figure 19 Diode Reverse Recovery Test Circuit

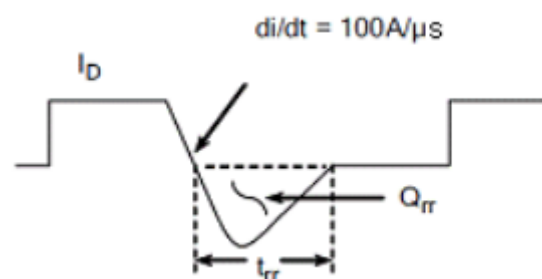


Figure 20 Diode Reverse Recovery Waveform

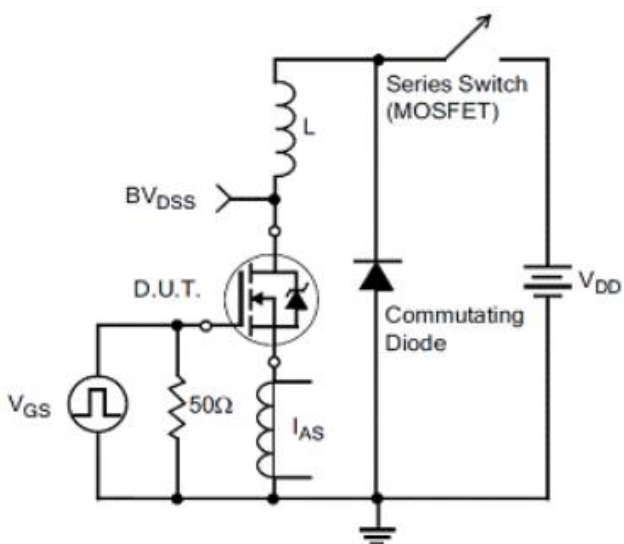


Figure 21 Unclamped Inductive Switching Test Circuit

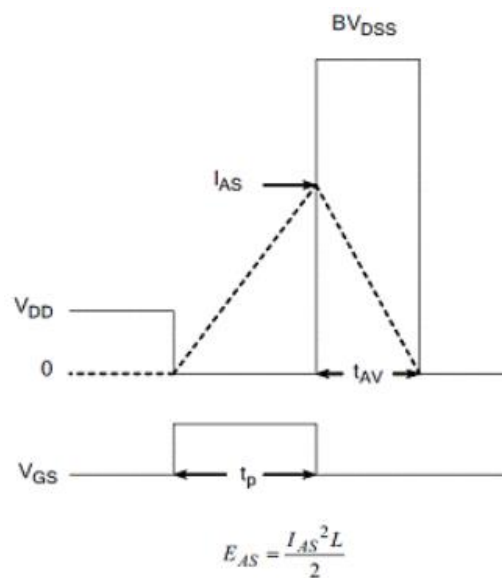
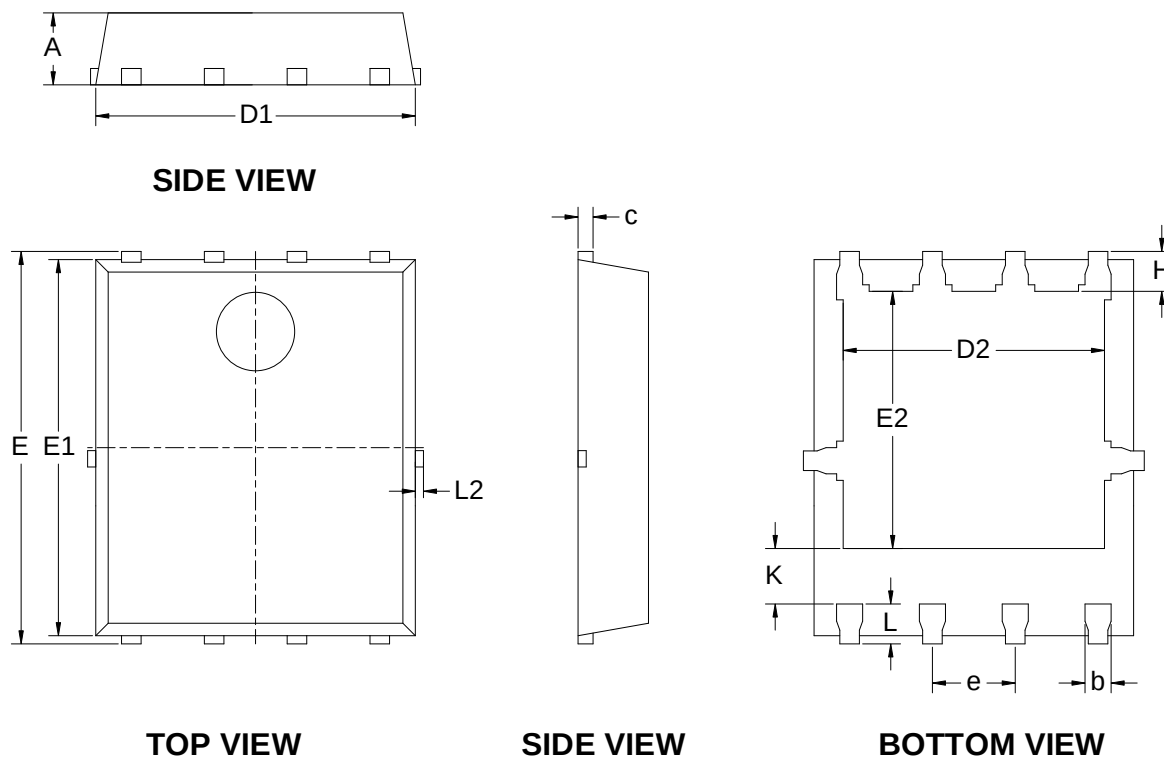


Figure 22 Unclamped Inductive Switching Waveform

8. Package Information

8.1 Package Outline Dimensions

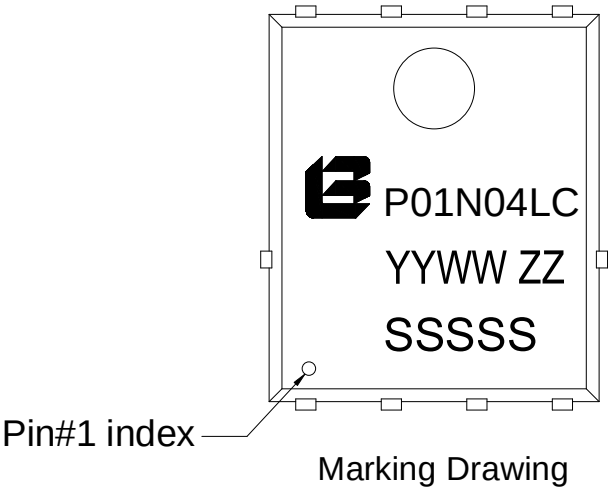
8.1.1 PDFN 5*6-8L



COMMON DIMENSION&TOLERANCE			
SYMBOL	ALL DIMENSION IN MILLIMETERS		
	MIN	MON	MAX
A	1.00	1.10	1.20
b	0.30	0.40	0.50
c	0.19	0.25	0.30
D1	4.80	5.00	5.20
D2	3.80	4.10	4.25
e	1.27 BSC		
E	5.90	6.15	6.25
E1	5.66	5.86	6.06
E2	3.28	3.48	3.68
H	0.50	0.65	0.75
K	1.00	1.30	1.50
L	0.50	0.64	0.74
L2	---	---	0.15

Unit: mm

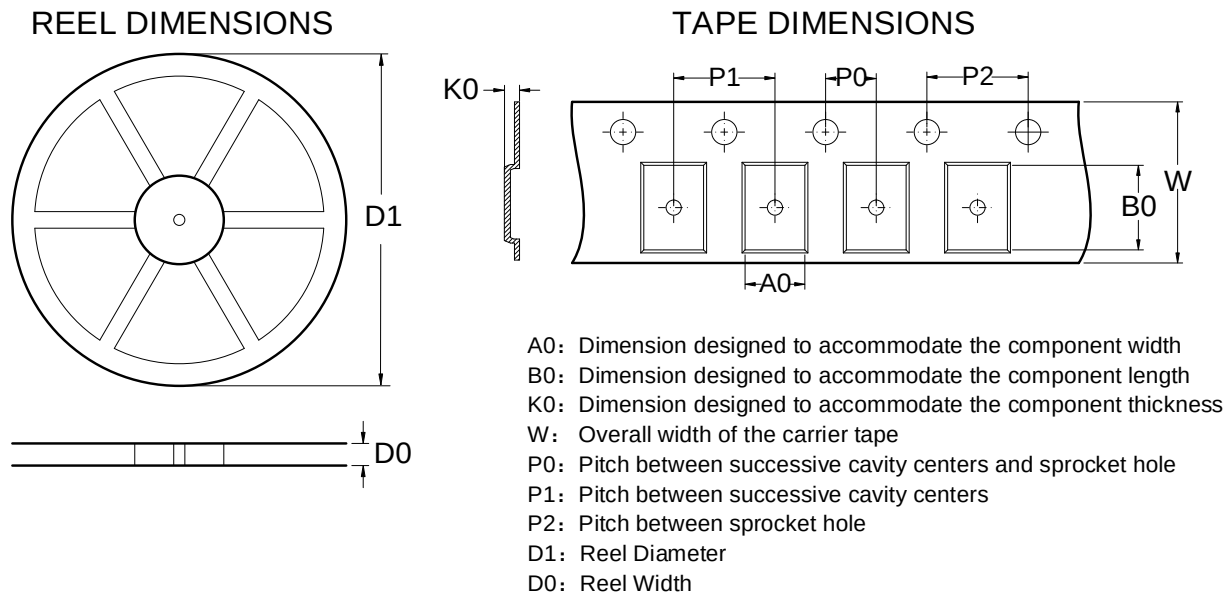
8.2 Marking



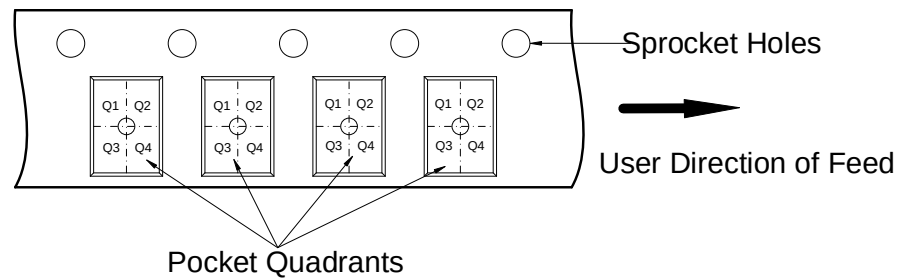
Content	Note
P01N04LC	Device Mark
YY	Calendar year code
WW	Workweek date code
ZZ	Assembly factory code
SSSSS	Lot ID

9. Packing specifications

9.1 PDFN 5*6-8L Reel Package



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

*All dimensions are nominal

Device	Package Type	Pins	SPQ	D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
BLP01N04LC-Q	PDFN5*6-8L	8	5000	330	12.4	6.55	5.84	1.4	2	8	4	12	Q1

Revision History

Revision	Date	Changes
Version 02	2025-12	Initial Version

Important Notice

- a. Exceeding Maximum Ratings: Operation beyond the device's maximum rated performance may result in damage to the device, including permanent failure, which could affect system reliability. Do not exceed the absolute maximum ratings during circuit design. Belling shall not be liable for any personal injury, property damage, or other adverse consequences arising from user misuse, including but not limited to incorrect operation, negligence, or similar circumstances.
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