

1. Description

BLQ3N100E, the silicon N-channel Enhanced MOSFETs, is obtained by advanced MOSFET technology which reduce the conduction loss, improve switching performance, and enhance the avalanche energy. The transistor is suitable device for SMPS, high speed switching and general purpose applications.

KEY CHARACTERISTICS

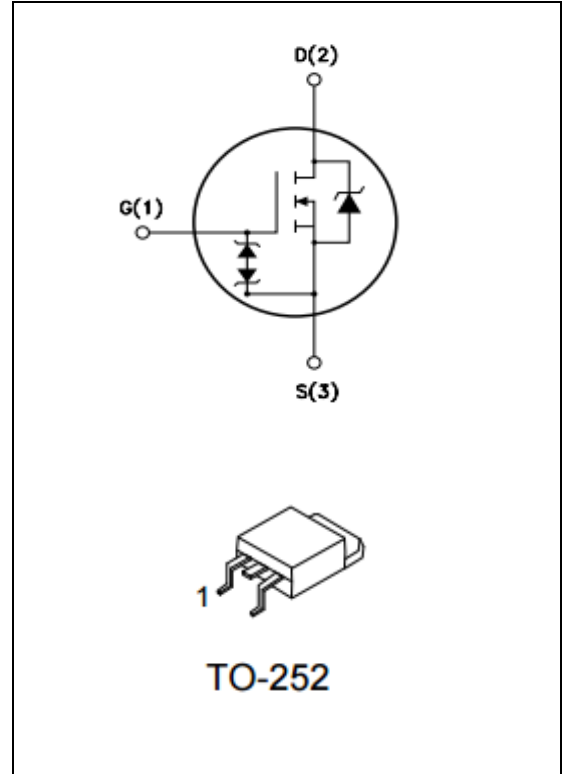
Parameter	Value	Unit
V_{DS}	1000	V
I_D	2.5	A
$R_{DS(ON).Typ}$	6.2	Ω

FEATURES

- Fast Switching
- Low C_{rss}
- 100% avalanche tested
- Improved dv/dt capability
- Zener - Protected
- RoHS product
- AEC-Q101 qualified

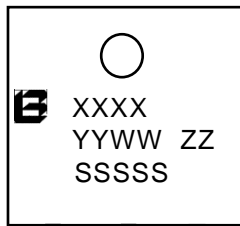
APPLICATIONS

- High frequency switching mode power supply



ORDERING INFORMATION

Ordering Codes	Package	Product Code	Packing
BLQ3N100E-D	TO-252	Q3N100E	Tape Reel

<p>BLQ3N100E-D</p> <div style="border: 1px solid black; padding: 5px; margin: 10px 0;"> (2) Package type (1) Chip name </div> <p>(1) BLQ3N100E:1000V 2.5A (2) D: TO-252</p>	<div style="border: 1px solid black; padding: 5px; margin: 10px 0;">  </div> <p>XXXX: Product Code YYWW: Year & Week ZZ: Assembly Code SSSS: Lot Code</p>
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2. ABSOLUTE RATINGS

at $T_c = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	1000	V
I_D	Continuous Drain Current	2.5	A
	Continuous Drain Current $T_c = 100^\circ\text{C}$	1.58	A
I_{DM}	Pulsed Drain Current(Note1)	10	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy(Note2)	200	mJ
$V_{ESD}(G-S)$	Gate source ESD (HBM, C=100pF, R=1.5k Ω)	3	kV
dv/dt	Peak Diode Recovery dv/dt(Note3)	5.0	V/ns
P_D	Power Dissipation, TO-252	62.5	W
	Derating Factor above 25°C	0.5	W/ $^\circ\text{C}$
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	$^\circ\text{C}$
T_L	Maximum Temperature for Soldering	300	$^\circ\text{C}$

3. Thermal characteristics

Symbol	Parameter	Package	RATINGS	Units
$R_{\theta JC}$	Junction-to-Case	TO-252	2.0	$^\circ\text{C}/\text{W}$

4. Electrical Characteristics

at $T_c = 25^\circ\text{C}$, unless otherwise specified

OFF Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	1000	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	$I_D=250\mu\text{A}$, Reference 25°C	--	0.75	--	V/ $^\circ\text{C}$
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=1000\text{V}$, $V_{GS}=0\text{V}$, $T_J=25^\circ\text{C}$	--	--	200	nA
		$V_{DS}=800\text{V}$, $V_{GS}=0\text{V}$, $T_J=125^\circ\text{C}$	--	--	10	μA
$I_{GSS}(F)$	Gate to Source Forward Leakage	$V_{GS}=+25\text{V}$	--	--	10	μA
$I_{GSS}(R)$	Gate to Source Reverse Leakage	$V_{GS}=-25\text{V}$	--	--	10	μA

ON Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10V$, $I_D=1.25A$ (Note4)	--	6.2	7.5	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu A$ (Note4)	3	--	5	V
g_{fs}	Forward Transconductance	$V_{DS}=15V$, $I_D = 2.5A$ (Note4)	2	--	--	S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
R_g	Gate resistance	$f = 1.0MHz$	--	4.5	--	Ω
C_{iss}	Input Capacitance	$V_{GS}=0V$ $V_{DS}=25V$ $f=1.0MHz$	--	530	--	PF
C_{oss}	Output Capacitance		--	45	--	
C_{rss}	Reverse Transfer Capacitance		--	2.5	--	
Q_g	Total Gate Charge	$I_D=2.5A$ $V_{DD}=450V$ $V_{GS}=10V$	--	13.8	--	nC
Q_{gs}	Gate to Source Charge		--	4.6	--	
Q_{gd}	Gate to Drain ("Miller") Charge		--	4.8	--	

Switching Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D = 2.5A$ $V_{DD} = 500V$ $V_{GS} = 10V$ $R_G = 5\Omega$ $T_J = 25^\circ C$	--	23	--	ns
t_r	Rise Time		--	63	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	33	--	
t_f	Fall Time		--	61	--	

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)	$T_C=25^\circ C$	--	--	2.5	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	10	A
V_{SD}	Diode Forward Voltage	$I_S=2.5A, V_{GS}=0V$ (Note4)	--	--	1.2	V
T_{rr}	Reverse Recovery Time	$I_S=2.5A, T_J = 25^\circ C$	--	2103	--	ns
Q_{rr}	Reverse Recovery Charge	$V_{GS}=0V, di_F/dt=100A/us$	--	1979	--	nC

Gate-source Zener diode						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
V _{GSO}	Gate-source breakdown voltage	I _{GS} = ±1mA (Open Drain)	30	--	--	V
The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source.						

Note1: Pulse width limited by maximum junction temperature

Note2: L=120mH, V_{DS}=50V, Start T_J=25°C

Note3: I_{SD} =3A, di/dt ≤100A/us, V_{DD}≤BV_{DSS}, Start T_J=25°C

Note4: Pulse width tp≤300μs, δ≤2%

5. Characteristics Curves

Figure 1 Safe Operating Area

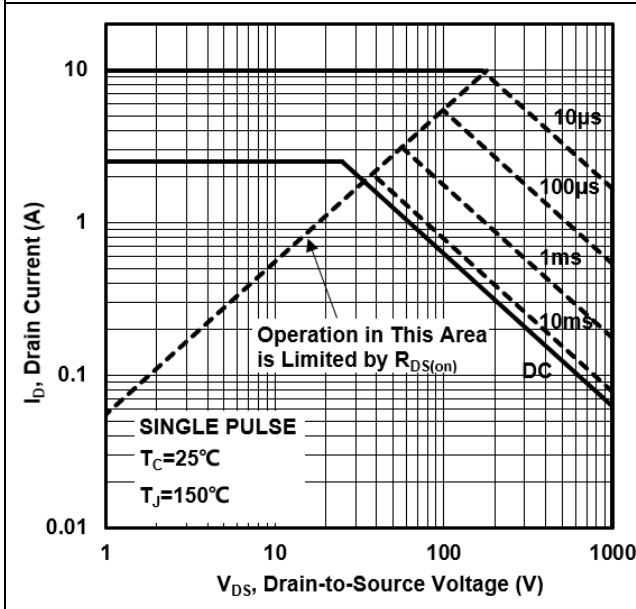


Figure 2 Power Dissipation

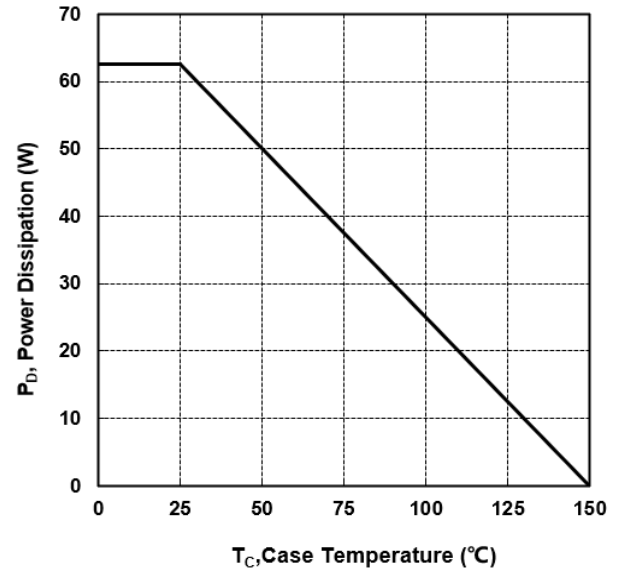


Figure 3 Typical Output Characteristics

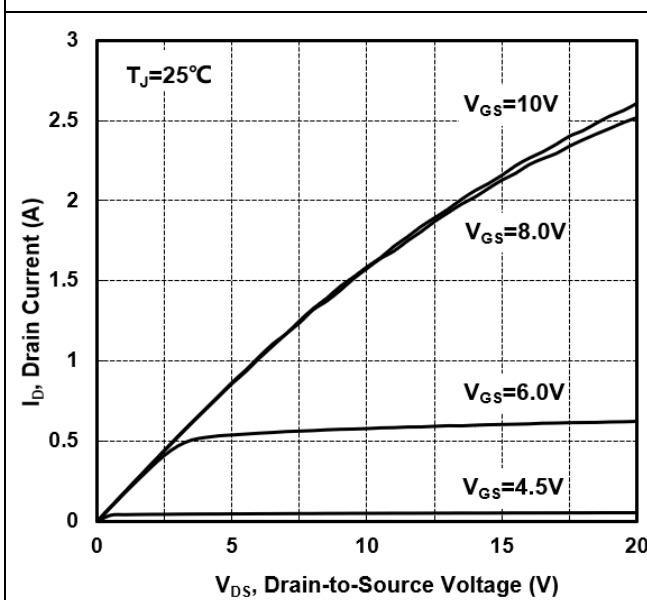


Figure 4 Typical Transfer Characteristics

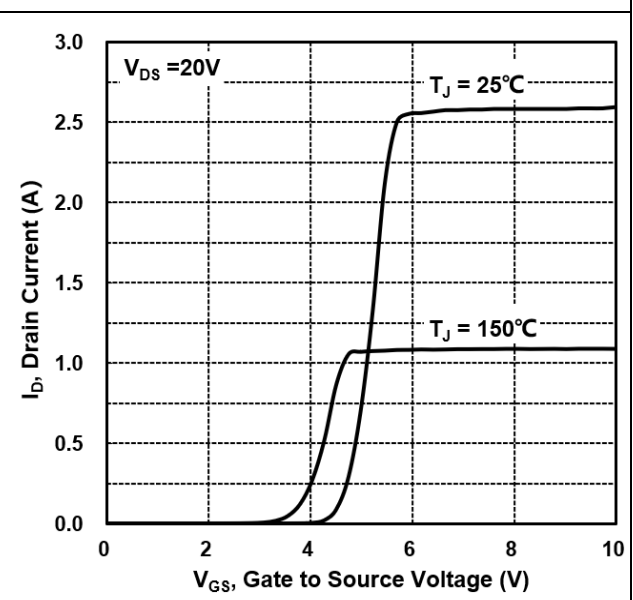


Figure 5 Typical Drain to Source ON Resistance vs Drain Current

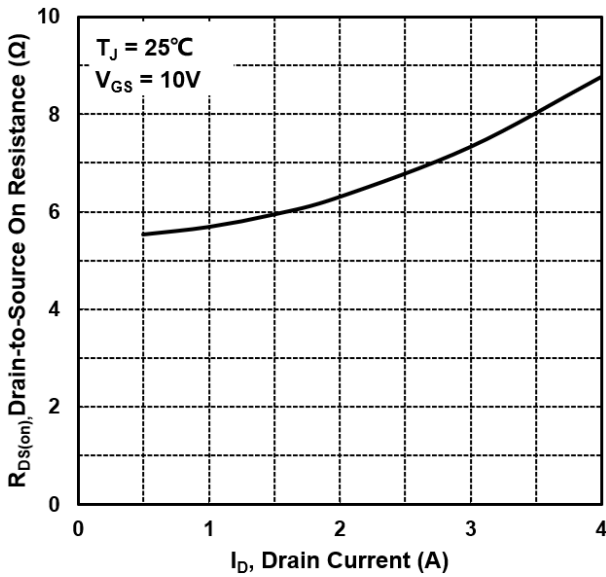


Figure 6 Typical Drain to Source on Resistance vs Junction Temperature

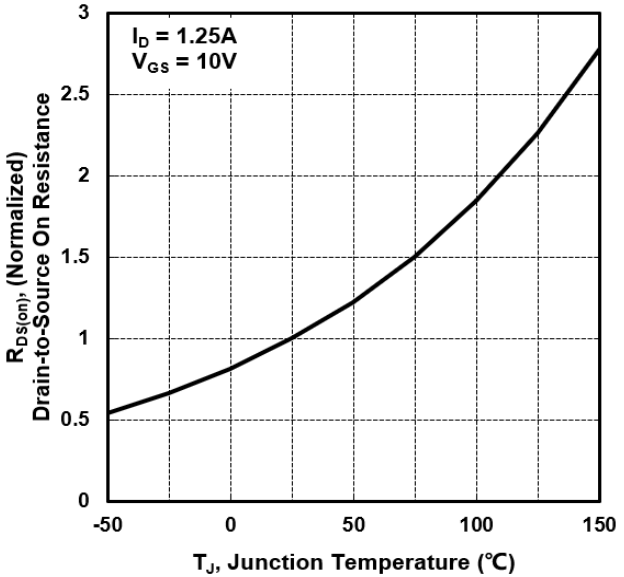


Figure 7 Typical Threshold Voltage vs Junction Temperature

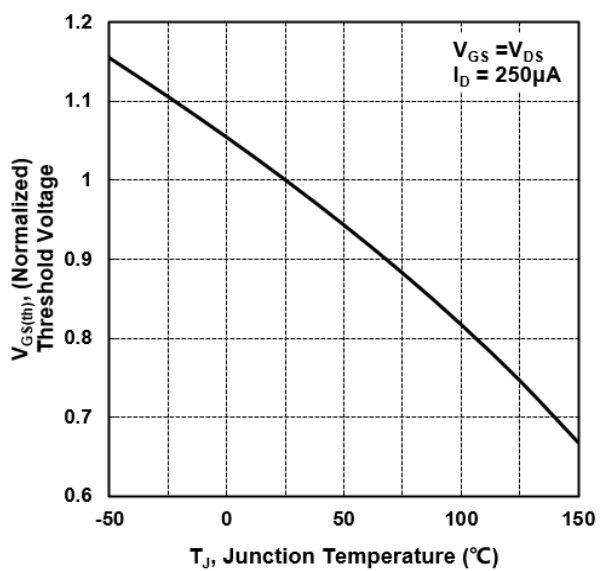


Figure 8 Typical Breakdown Voltage vs Junction Temperature

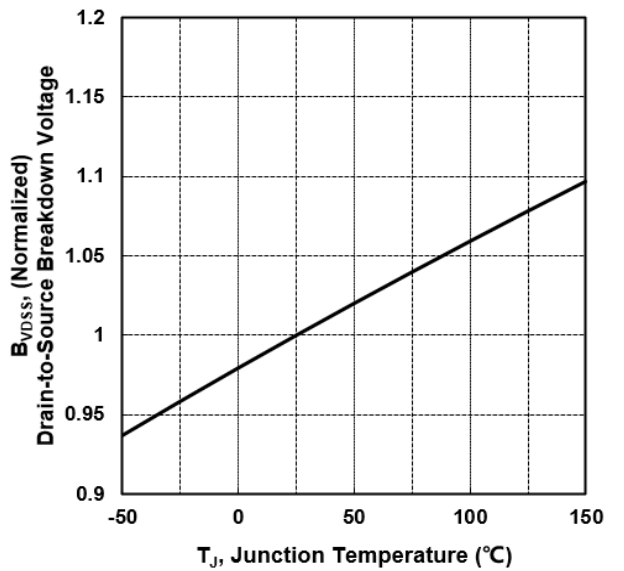


Figure 9 Typical Capacitance vs Drain to Source Voltage

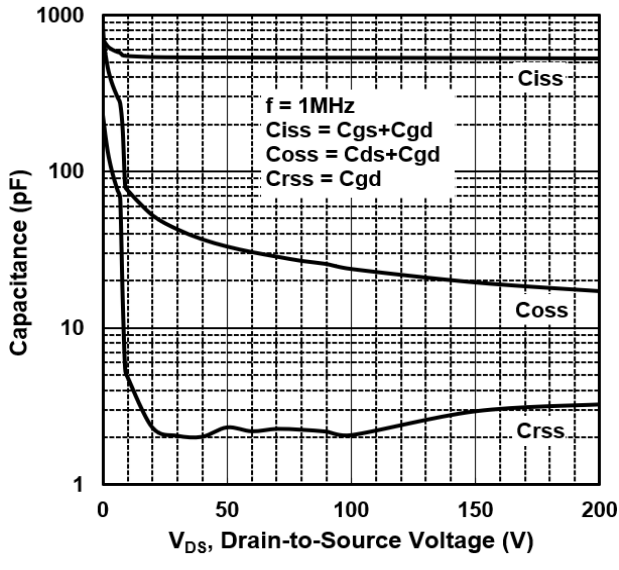


Figure 10 Typical Gate Charge vs Gate to Source Voltage

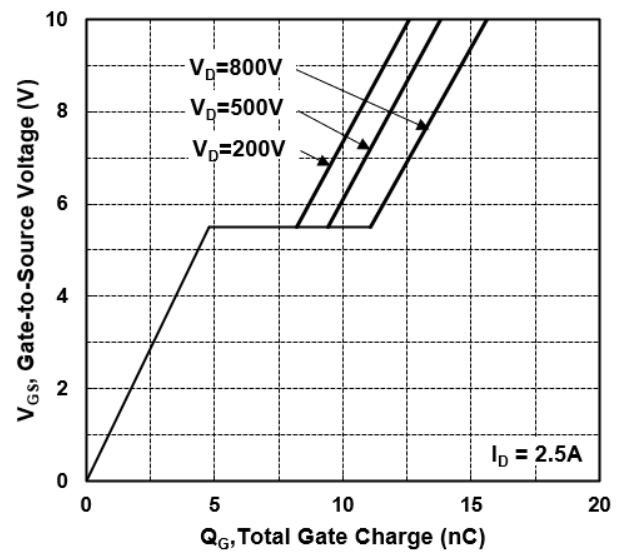
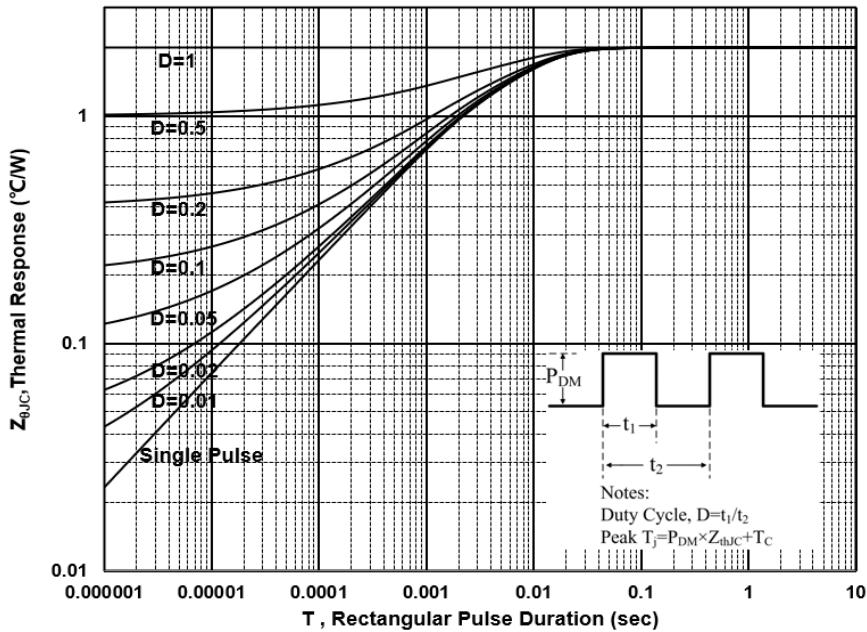


Figure 11 Transient Thermal Impedance, Junction to Case



6. Test Circuit and Waveform

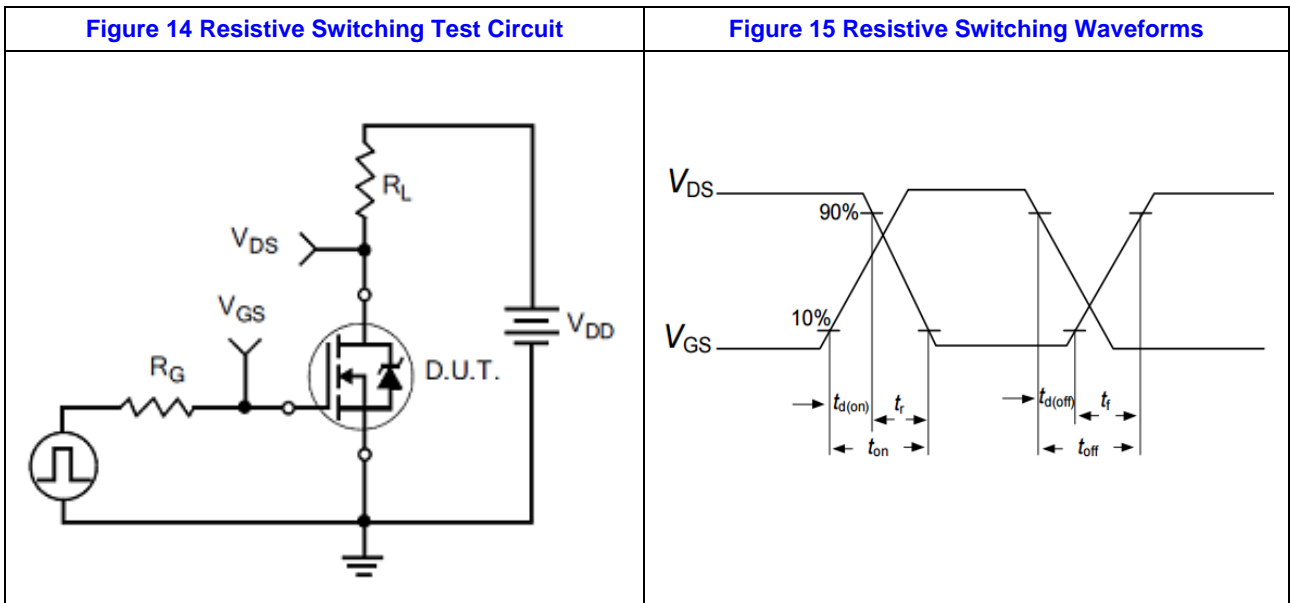
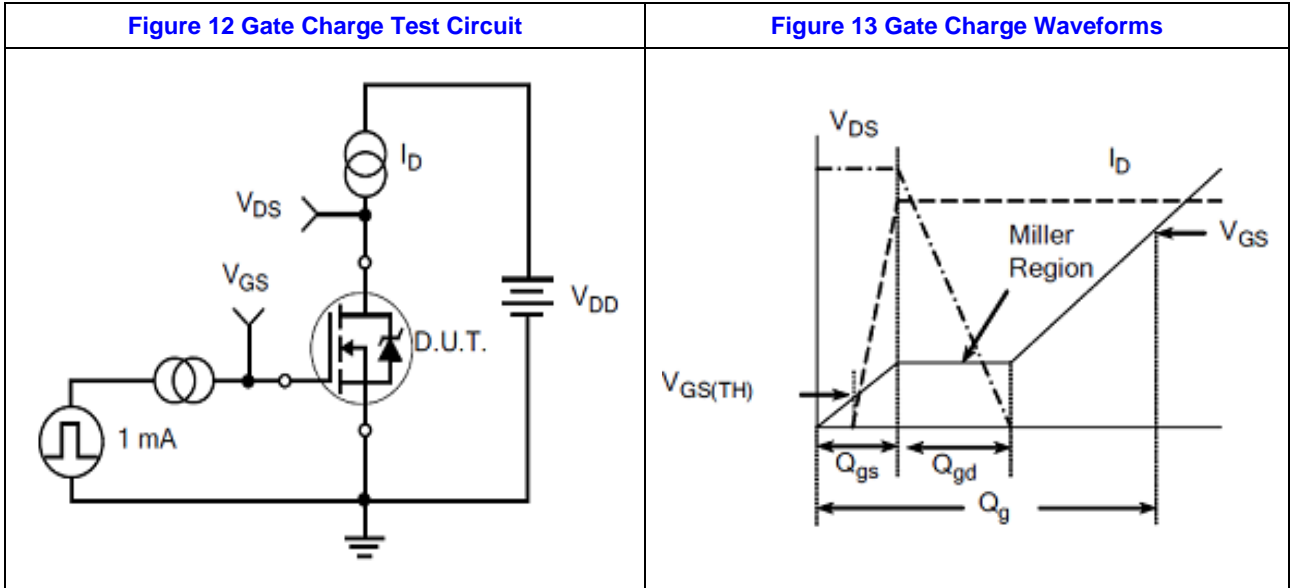


Figure 16 Diode Reverse Recovery Test Circuit

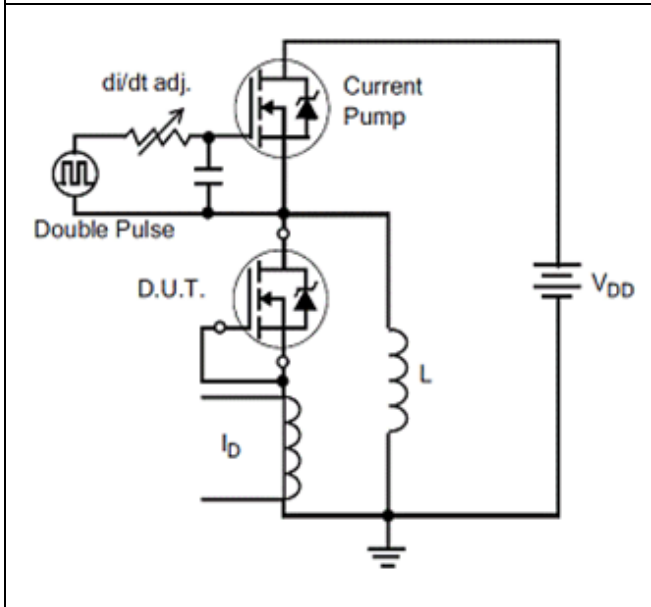


Figure 17 Diode Reverse Recovery Waveform

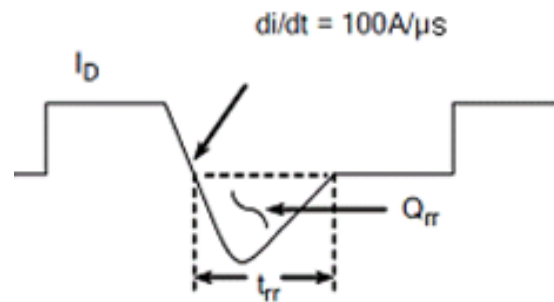


Figure 18 Unclamped Inductive Switching Test Circuit

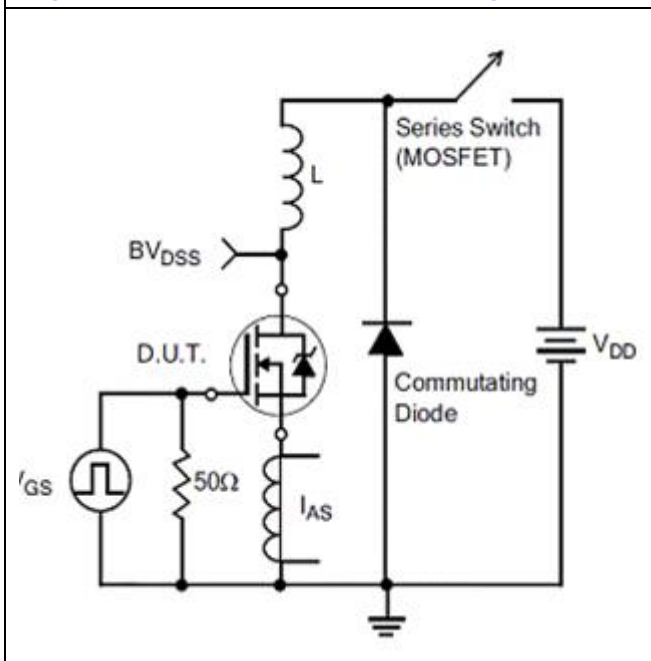
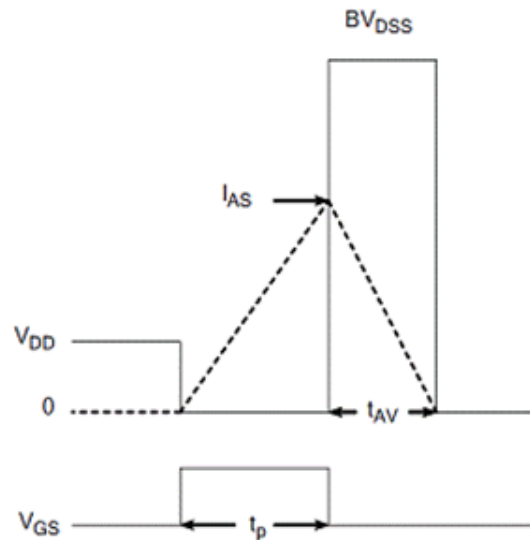
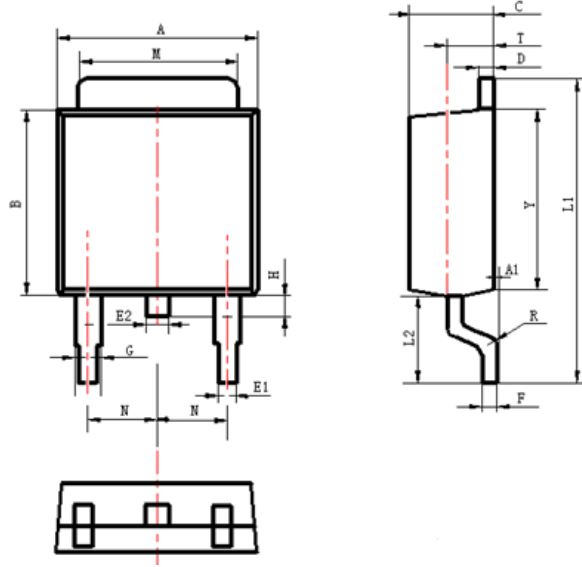


Figure 19 Unclamped Inductive Switching Waveform



7. Package Description



Items	Values(mm)	
	MIN	MAX
A	6.30	6.90
A1	0	0.13
B	5.70	6.30
C	2.10	2.50
D	0.30	0.60
E1	0.60	0.90
E2	0.70	1.00
F	0.30	0.60
G	0.70	1.20
L1	9.60	10.50
L2	2.70	3.10
H	0.60	1.00
M	5.10	5.50
N	2.09	2.49
R	0.3	
T	1.40	1.60
Y	5.10	6.30

TO-252 Package

Revision History:

BLQ3N100E Revision: 2024-12-29, Rev. 1.1

Previous Revision

Revision	Date	Revision Date Subjects (major changes since last revision)
1.0	2023-02-24	
1.1	2024-12-29	Improve IDSS SPEC

We Listen to Your Comments

If there is any information within this document that you feel is wrong, unclear, or missing at all, please contact us.

Your feedback will help us to continuously improve the quality of this document.

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NOTE:

1. Any use beyond the maximum ratings of the device in performance may cause damage to the device or even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when designing circuit.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. Semiconductor device is sensitive to the ESD, it is necessary to protect the device from being damaged by the ESD when using it.
4. Shanghai Belling reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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